CIO-DDA06
Analog Output Board

User's Manual

Revision 6
September, 2000

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1.0 INTRODUCTION

The CIO-DDA06 has six channels of analog output and 24 digital inputs/outputs. The analog outputs are dual-DAC AD7273s with each output buffered by an OP07. The heart of the digital I/O is one 82C55. The CIO-DDA06 is 100% compatible with MetraByte's DDA-06.

The analog outputs are controlled by writing a digital control word as two bytes to the DAC's control register. The control register is double buffered so the DAC's output is not updated until both bytes (first low byte, then high byte) have been written to the DAC control when the simultaneous transfer jumper is in the default UPDATE position.

The analog outputs may also be set for simultaneous update in groups of two, four, or all six. Analog outputs are grouped as 0&1, 2&3 and 4&5. By selecting XFER on the jumper below the DAC, each pair may be set for simultaneous update.

When a DAC pair is set for simultaneous update, writing new digital values to the DAC's control register does not cause an update of the DAC's voltage output. Update of the output occurs only after a READ from the board's address (any address base + 0 through base + B).

In this way, the CIO-DDA06 may be set to hold new values until all channels are loaded, then update any two, four, or all six channels simultaneously. This is a very handy feature for multi-axis motor control.

The CIO-DDA06 digital I/O lines are a direct interface to an 82C55. The 82C55 is a CMOS chip with TTL level inputs and outputs. The 8255 can source or sink about 2.5 mA. This is adequate to switch other TTL or similar inputs, but is inadequate to drive relays, LEDs or solid state relays.

The CIO-DDA06 digital I/O is controlled by programming the 8255's mode register. There are three possible modes. The simplest and most commonly used mode is mode 0, simple input and output.

2.0 SOFTWARE INSTALLATION

Before you open your computer and install the board, install and run *Insta*Cal, the installation, calibration and test utility included with your board. If you have ordered the Universal Library, *Insta*Cal can be installed from that disk set rather than the *Insta*Cal disk set. Refer to the *Software Installation* manual for *Insta*Cal installation instructions.

*Insta*Cal will guide you through switch and jumper settings for your board. Detailed information regarding these settings can be found below. After configuring your board, install it in your computer as detailed in the Hardware Installation section below and run *Insta*Cal. Once you have restarted your computer, run *Insta*Cal and installed your board, use *Insta*Cal to verify your installation and switch settings.

3.0 HARDWARE INSTALLATION

The CIO-DDA06 has a bank of six switches for setting the base address, six banks of five switches for setting the gain for each DAC, three simultaneous transfer jumpers, a "power-up state" jumper and one wait state jumper block. These switches may require setting before installing the board in your computer. This manual and the installation program (InstaCal) included with the board describes how these switches are set. In addition, each analog channel has a gain and an offset potentiometer for calibrating the channel if necessary.

The CIO-DDA06 is configured at the factory with the following hardware settings (Table 3-1):

Table 3-1. Factory-Set Default Settings

BASE ADDRESS	300H (768 Decimal)
WAIT STATE	Off position, Right
SIMULTANEOUS TRANSFER JUMPER	In the UPDATE position. Single channel update
ANALOG OUTPUT RANGE	+/-5V
POWER UP STATE	Standard mode

Leave the switches as they were set at the factory or refer to this manual to change the settings. They are described in this manual.

3.1 BASE ADDRESS

The base address is the starting location that software writes to when communicating with the CIO-DDA06. A set of DIP switches is used for setting the base address. By placing the switch down, the CIO-DDA06 address decode logic is instructed to respond to that address bit. A complete address is constructed by calculating the HEX or decimal number which corresponds to all the address bits the board has been instructed to respond to. For example, in Figure 3-1, for address 300h, switches 9 and 8 are DOWN, all others UP. Switch 9 = 200h (512D) and switch 8 = 100h (256D), when added together they equal 300h (768D).

NOTE
DISREGARD THE NUMBERS PRINTED ON THE SWITCH. REFER TO THE NUMBERS PRINTED IN WHITE ON THE BOARD.

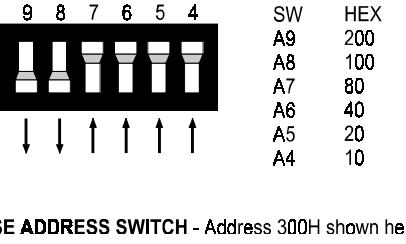


Figure 3.1 Base Address Switches

Unless there is already a board in your system which uses address 300h (768 Decimal), leave the switches as they are set at the factory (Figure 3-1).

3.2 WAIT STATE JUMPER

The CIO-DDA06 boards have a wait state jumper which can enable an on-board wait state generator (Figure 3-2). A wait state is an extra delay injected into the processor's clock via the bus. This delay slows down the processor when the processor addresses the CIO-DDA06 board so that signals from slow devices (chips) will be valid

The wait state generator on the CIO-DDA06 is only active when the CIO-DDA06 is being accessed. Your PC will not be slowed down in general by using the wait state.

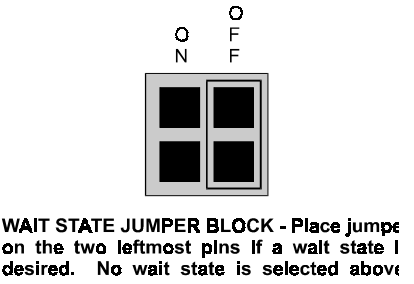


Figure 3-2. Wait State Jumper

3.3 SIMULTANEOUS TRANSFER JUMPER

The analog outputs can be jumpered so that new output data is held until several DACs have been loaded with new digital data. Then, as a group, the data for each DAC is simultaneously transferred and the DAC voltage outputs are updated when when any of the addresses BASE + 0 to BASE + B are read.

The analog output chips on the CIO-DDA06 are dual DACs. Two analog outputs are on each chip. A single jumper sets both DACs on a single chip to be individual UPDATE or simultaneous TRANSFER.

The diagram in Figure 3-3 below shows the jumper block in each configuration. If you look on the CIO-DDA06 board, you will see the numbers 45, 23, and 01 (left to right) next to the simultaneous transfer jumpers. Those numbers indicate which channels that jumper selects (0 and 1, 2 and 3, 4 and 5).

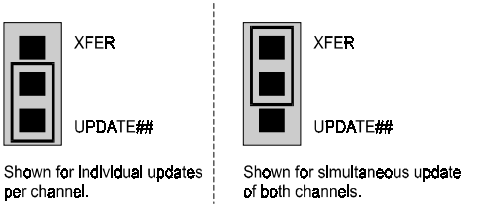


Figure 3-3. Simultaneous Transfer Jumpers.

3.4 POWER UP STATE JUMPER

The analog outputs may be jumpered so that their power up state is 0V. A single jumper sets this option for all six channels. In the zero volts mode, “ZERO”, they are held at 0V until one of the DAC “Most Significant Nibble” registers is written to and then any of the DAC registers are read. In the standard mode, “STD”, they power up in an undetermined state.

Figure 3-4 below shows the jumper in each configuration.

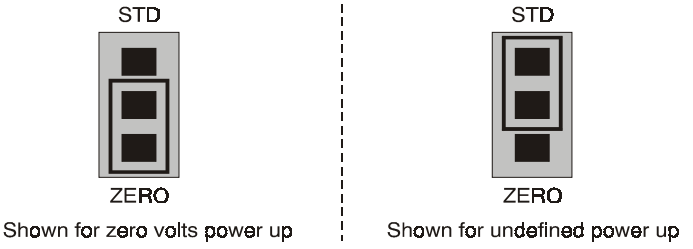
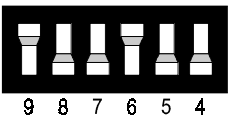


Figure 3-4. Power-Up State Jumper

3.5 ANALOG OUTPUT RANGE SWITCH

The analog output voltage range of each channel can be set via a six position DIP switch. The switches are located on the board directly below the calibration potentiometers and are labeled GAIN 5 through GAIN 0.



OUTPUT RANGE SWITCH - One per channel.
Factory default +/-5V shown here.

Figure 3-5 Analog Output Range Switch

Set the switches for an individual channel as shown here.

RANGE						
+/-10	UP	DN	UP	DN	DN	DN
+/-5	UP	DN	DN	UP	DN	DN
+/-2.5	UP	DN	DN	DN	UP	DN
+/-1.67	UP	DN	DN	DN	DN	UP
0 to 10	DN	UP	UP	DN	DN	DN
0 to 5	DN	UP	DN	UP	DN	DN
0 to 2.5	DN	UP	DN	DN	UP	DN
0 to 1.67	DN	UP	DN	DN	DN	UP

To set a chosen range, read the switch positions as UP or DN (down) from left to right in the row beside the range you desire.

For example, the 5V bipoar range is: UP - DN - DN - UP - DN - DN.

3.6 INSTALLING THE CIO-DDA06 IN THE COMPUTER

1. Turn the power off.

2. Remove the cover of your computer. Please be careful not to dislodge any of the cables installed on the boards in your computer as you slide the cover off.

3. Locate an empty expansion slot in your computer. Push the board firmly down into the expansion bus connector. If it is not seated fully it may fail to work and could short circuit the PC bus power onto a PC bus signal. This could damage the motherboard in your PC as well as the CIO-DDA06.

3.7 CABLING TO THE CIO-DDA06

The CIO-DDA06 connector is accessible through the PC/AT expansion bracket. The connector is a standard 37 pin male connector. A mating female connector or C37FF-# cable can be purchased from the manufacturer. Several cabling, screw termination, and signal conditioning options are available including:

DFCON-37	D connector, D shell and termination pins to contruct your own cable.
C37FF-#	2 foot (and longer) ribbon cable with 37 pin D-type female connectors.
C37FFS-#	5 foot and 10 foot shielded round cable with molded ends housing 37 pin female connectors.
CIO-MINI37	Simple, 40 position 4”x4” screw terminal board.
SCB-37	A metal enclosure housing two CIO-MINI37 screw terminal boards
CIO-TERMINAL	Full featured 4”x16” screw terminal board with prototyping and interface circuitry.
SSR-RACK24	24 position Solid State Relay mounting and interface board.
ISO-RACK08	8 position Isolated Analog Module mounting and interface board.
ENC-MINI37	Enclosure for the MINI37.
ENC-17-3	Enclosure for larger external accessory boards.

3.8 SIGNAL CONNECTION

The analog outputs of the CIO-DDA06 are two-wire hook-ups. A signal, labeled D/A # OUT on the connector diagram below, and a Low Level Ground (LLGND). The low level ground is an analog ground and is the ground reference which should be used for all analog hook-ups.

Analog output ranges are:

Bipolar Ranges	+/-10V	+/-5V	+/-2.5V	+/-1.67V
		and		
Unipolar Ranges	0 to 10V	0 to 5V	0 to 2.5V	0 to 1.67V

All the digital outputs inputs on the CIO-DDA06 connector are TTL level. Before connecting external devices, review the specifications in this manual to avoid damage to the CIO-DDA06.

3.9 CONNECTOR DIAGRAM

The CIO-DDA06 connector is a 37-pin D-type connector accessible from the rear of the PC through the expansion backplate (Figure 3-6). The connector accepts female 37-pin D-type connectors,such the C37FF-2, a two-foot cable with two female connectors. If frequent changes to signal connections are required or if signal conditioning is needed, please refer back to Section 3.7

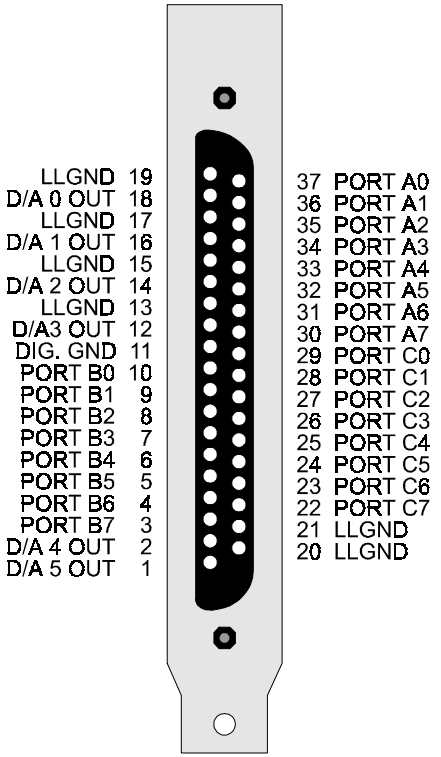


Figure 3-6. 37-Pin Connector Pin-Out

4.0 CALIBRATION

A calibration option is supplied with InstaCal. If desired, run CALIBRATE and check the calibration of the board. This step may not be necessary since the board was calibrated at the factory.

5.0 ARCHITECTURE & REGISTERS

All control and data is read/written with simple I/O read and write signals. No interrupt or DMA control software is required. The board's functions are easy to control directly from BASIC, C, or PASCAL.

The board consists of two separate function blocks, analog and digital. The digital block consists of a single 82C55, 24 line digital I/O chip. The analog block consists of three identical circuits, each comprised of one dual DAC, two OP07 output buffers and range control. Each of the analog outputs can be individually controlled, or groups of 2, 4 or all 6 outputs can be controlled simultaneously.

5.1 CONTROL & DATA REGISTERS

The CIO-DDA06 has 12 analog output registers. There are two registers for each analog output channel, one for the lower 8 bits and one for the upper 4 bits. An additional four addresses are used for the 82C55 data (3) and control (1) registers. The board occupies 16 I/O addresses in all. The registers and their function are listed on Table 5-2.

The first address, or BASE ADDRESS, is determined by setting a bank of switches on the board.

Register manipulation is best left to experienced programmers as most of the CIO-DDA06 possible functions are implemented in Measurement Computing's easy to use Universal Library.

The register descriptions all follow the format:

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Where the numbers along the top row are the bit positions within the 8 bit byte and the numbers and symbols in the bottom row are the functions associated with that bit.

To write to or read from a register in decimal or HEX, the following weights apply:

Table 5-1 Bit Weights

BIT POSITION	DECIMAL VALUE	HEX VALUE
0	1	1
1	2	2
2	4	4
3	8	8
4	16	10
5	32	20
6	64	40
7	128	80

Table 5-2 Board Registers

ADDRESS	WRITE FUNCTION	READ FUNCTION
BASE + 0	D/A 0 Least Significant Byte	Initiate simultaneous transfer Enable DACs
BASE + 1	D/A 0 Most Significant Nibble	Initiate simultaneous transfer Enable DACs
BASE + 2	D/A 1 Least Significant Byte	Initiate simultaneous transfer Enable DACs
BASE + 3	D/A 1 Most Significant Nibble	Initiate simultaneous transfer Enable DACs
BASE + 4	D/A 2 Least Significant Byte	Initiate simultaneous transfer Enable DACs
BASE + 5	D/A 2 Most Significant Nibble	Initiate simultaneous transfer Enable DACs
BASE + 6	D/A 3 Least Significant Byte	Initiate simultaneous transfer Enable DACs
BASE + 7	D/A 3 Most Significant Nibble	Initiate simultaneous transfer Enable DACs
BASE + 8	D/A 4 Least Significant Byte	Initiate simultaneous transfer Enable DACs
BASE + 9	D/A 4 Most Significant Nibble	Initiate simultaneous transfer Enable DACs
BASE + 10	D/A 5 Least Significant Byte	Initiate simultaneous transfer Enable DACs
BASE + 11	D/A 5 Most Significant Nibble	Initiate simultaneous transfer Enable DACs
BASE + 12	Port A Output of 8255	Port A Input of 8255
BASE + 13	Port B Output	Port B Input
BASE + 14	Port C Output	Port C Input
BASE + 15	8255 Control Register	None

5.2 ANALOG REGISTERS

BASE ADDRESS +0 through +11

WRITE
Loading all DAC registers with the desired value is the first step in enabling the outputs when the "Zero" power up mode is set. Once all registers are loaded with the desired value, a READ of any DAC register will enable all DAC outputs and the voltage determined by the loaded values will appear at the outputs. After the first read, all outputs remain enabled until the board is reset (the PC is turned off or rebooted).

READ
Reading these registers is the second step in enabling the DAC outputs when the "Zero" powerup mode is set. A read is also required for triggering a simultaneous update. Enabling the outputs in “Zero” powerup mode and triggering a simultaneous update are very similar except that if not in simultaneous mode, only one read is required to enable the DAC outputs for “Zero” powerup mode. When in simultaneous update mode, a read is required for every update of the DAC outputs.

NOTE: Even if you are not using the simultaneous update feature, you must perform one read to enable the DAC outputs if you are using the "ZERO" power up mode feature.

5.3 ANALOG OUTPUT REGISTERS

D/A 0 LEAST SIGNIFICANT 8 BITS
BASE ADDRESS + 0

7	6	5	4	3	2	1	0
D5	D6	D7	D8	D9	D10	D11	D12 (LSB)

D/A 0 MOST SIGNIFICANT 4 BITS
BASE ADDRESS + 1

7	6	5	4	3	2	1	0
X	X	X	X	D1 (MSB)	D2	D3	D4

Writing data to the LSB loads that data into the D/A load register but does not update the D/A output. Writing data to the MSB both loads the upper 4 bits of the 12 bit digital value and updates the output of the D/A (when operating in STD mode).

The function and bit layout of the remaining 10 registers (5 D/As) is identical to that shown above.

5.4 DIGITAL I/O REGISTERS

PORT A DATA
BASE ADDRESS + 12

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

PORT B DATA
BASE ADDRESS + 13

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

Ports A & B can be programmed as input or output. Each is written to and read from in bytes, although for control and monitoring purposes, individual bits are used. Bit read and write functions require that unwanted bits be masked out of reads and ORed into writes.

PORT C DATA
BASE ADDRESS + 14

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0
CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

Port C may be used as one 8 bit port of either input or output, or it may be split into two 4 bit ports which may be independently input or output. The notation for the upper 4 pit port is CH3 - CH0, and for the lower, CL3 - CL0.

Although it may be split, every read and write to port C carries eight bits of data so unwanted information must be ANDed out of reads, and writes must be ORed with the current status of the other port.

OUTPUT PORTS
In 8255 mode 0 configuration, ports configured for output hold the output data written to them. This output byte can be read back by reading a port configured for output.

INPUT PORTS
In 8255 mode 0 configuration, ports configured for input read the state of the input lines at the moment the read is executed, transitions are not latched.

For information on modes 1 (strobed I/O) and 2 (bi-directional strobed I/O), refer to the manufacturer's data sheet.

8255 CONTROL REGISTER
BASE ADDRESS + 15

7	6	5	4	3	2	1	0
MS	M3	M2	A	CH	M1	B	CL
	Group A				Group B		

The 8255 can be programmed to operate in Input/ Output (mode 0), Strobed Input/ Output (mode 1) or Bi-Directional Bus (mode 2).

When the PC is powered up or RESET, the 8255 is reset. This places all 24 lines in Input mode and no further programming is needed to use the 24 lines as TTL inputs.

To program the 8255 for other modes, the following control code byte must be assembled into one eight-bit byte.

MS = Mode Set. 1 = mode set active

Table 5-3. 82C55 Mode Control Coding

MS	**M3**	**M2**	**Group A Function**
1	0	0	Mode 0 Input / Output
1	0	1	Mode 1 Strobed Input / Output
1	1	X	Mode 2 Bi-Directional Bus

If all ports are to be used for either all inputs or for all outputs, the A, B, CH, and CL set the bits set as in Table 5-4 below.

Table 5-4. Coding for All inputs or All Outputs

A	B	CL	CH	I/O Function
1	1	1	1	All Inputs
0	0	0	0	All Outputs

M1 = 0 is mode 0 for group B. Input / Output
M1 = 1 is mode 1 for group B. Strobed Input / Output

The Ports A, B, C High and C Low can be independently programmed for input or output. The two groups of ports, group A and group B, can be independently programmed in one of several modes. The most commonly used mode is mode 0, input / output mode. The codes for programming the 8255 in this mode are shown below.

Table 5-5. Digital I/O Configuration

A	CH	B	CL	D4	D3	D1	D0	HEX	DEC
OUT	OUT	OUT	OUT	0	0	0	0	80	128
OUT	OUT	OUT	IN	0	0	0	1	81	129
OUT	OUT	IN	OUT	0	0	1	0	82	130
OUT	OUT	IN	IN	0	0	1	1	83	131
OUT	IN	OUT	OUT	0	1	0	0	88	136
OUT	IN	OUT	IN	0	1	0	1	89	137
OUT	IN	IN	OUT	0	1	1	0	8A	138
OUT	IN	IN	IN	0	1	1	1	8B	139
IN	OUT	OUT	OUT	1	0	0	0	90	144
IN	OUT	OUT	IN	1	0	0	1	91	145
IN	OUT	IN	OUT	1	0	1	0	92	146
IN	OUT	IN	IN	1	0	1	1	93	147
IN	IN	OUT	OUT	1	1	0	0	98	152
IN	IN	OUT	IN	1	1	0	1	99	153
IN	IN	IN	OUT	1	1	1	0	9A	154
IN	IN	IN	IN	1	1	1	1	9B	155

Note: D7 is always 1.
D6, D5 and D2 are always 0.

5.5 OPTIONAL DC/DC CONVERTER

An optional DC/DC converter may be installed by Measurement Computing. The DC/DC converter provides +/-15V, eliminating the need for the +/-12V supply of the PC.

This option is useful only to those who wish to install the CIO-DDA06 in a PC that does not have both 12V, such as a portable.

This option must be specified at the time of order by adding a CIO-PG408 to the order.

6.0 SPECIFICATIONS

POWER CONSUMPTION

+5V	435 mA typical, 525 mA max
+12V	50 mA typical, 80 mA max
−12V	120 mA typical, 160 mA max

With optional DC/DC converter installed:

+5V	935 mA typical / 1.025A max
+12V	N/A
−12V	N/A

ANALOG OUTPUT

D/A convertor type	AD7237
Resolution	12 bits
Number of channels	6
Output Ranges	±10V, ±5V, ±2.5V, ±1.67V, 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.67. Each channel independently switch selectable.
D/A pacing	Software paced
D/A trigger modes	Software
Data transfer	Programmed I/O
Offset error	Trimmable to zero
Gain error	Trimmable to zero
Differential nonlinearity	± ½LSB max
Integral nonlinearity	± ½LSB max
Monotonicity	± ½LSB max
D/A Gain drift	±15 ppm/°C typical, ±30 ppm/°C max
D/A Bipolar offset drift	±7 ppm/°C typical, ±15 ppm of FSR/°C max
D/A Unipolar offset drift	±1 ppm/°C typical, ±3 ppm of FSR/°C max
Throughput	System dependent
Output Slew Rate	5V/µS
D/A Settling time (20V step to ±0.01%)	5µs typ, 10µs max
D/A Slew Rate	<4V/µs
Current Drive	±5 mA
Output short-circuit current	20 mA indefinite
Output coupling	DC
Output impedance	0.1 Ohms max
Miscellaneous	Double buffered output latches

	Update DACs individually or simultaneously (jumper selectable by pairs) Power up and reset option, jumper selectable (revision 3 and up): With jumper set to “ZERO”, all DAC's cleared to 0 volts, ±32mV, DACs set to simultaneous update mode until first read; With jumper set to STD, DAC output on power-up is undefined

DIGITAL INPUT / OUTPUT

Digital Type	82C55
Configuration	2 banks of 8, 2 banks of 4, programmable by bank as input or output
Number of channels	24 I/O
Output High	3.0 volts min @ –2.5mA
Output Low	0.4 volts max @ 2.5mA
Input High	2.0 volts min, 5.5 volts absolute max
Input Low	0.8 volts max, –0.5 volts absolute min
Power-up / reset state	Input mode (high impedance)

ENVIRONMENTAL

Operating temperature range	0 to 50°C
Storage temperature range	–20 to +70°C
Humidity	0 to 90% non-condensing

For Your Notes

For Your Notes

For Your Notes

Declaration of Conformity

We, Measurement Computing Corp., declare under sole responsibility that the product:

CIO-DDA06	Analog Output Board
Part Number	Description

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

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