CIO-DAS1601/12
CIO-DAS1602/12
CIO-DAS1602/16

ANALOG & DIGITAL I/O BOARD for ISA BUS

Standard and -P5 versions

MEASUREMENT COMPUTING™

Revision 6

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1 INTRODUCTION

The installation and operation of all CIO-DAS1600 series boards are very similar. Throughout this manual we use CIO-DAS1600 as a generic designation for the CIO-DAS1601/12, CIO-DAS1602/12, and CIO-DAS1600/16. When required, due to the differences in the boards, the specific board name is used.

2 SOFTWARE INSTALLATION

We recommend you install and run the ***InstaCal*™** installation, test and calibration utility that was shipped with your board prior to installing the board in your computer. ***InstaCal*™** will show you how to properly set the switches and jumpers on the board prior to physically installing the board in your computer.

Refer to the *Software Installation Manual* for detailed instructions regarding the installation of the ***InstaCal*™** software.

3 HARDWARE INSTALLATION

The CIO-DAS1600 has a variety of switches and jumpers to set before installing the board in your computer. By far the simplest way to configure your board is to use the ***Insta*Cal™** program provided as part of your CIO-DAS1600 software package. ***Insta*Cal™** will show you all available options, how to configure the various switches and jumpers to match your application requirements, and will create a configuration file that your application software (and the Universal Library) will refer to so the software you use will automatically know the exact configuration of the board.

Please refer to the *Software Installation Manual* regarding the installation and operation of ***Insta*Cal™**. The following hard copy information is provided as a matter of completeness, and will allow you to set the hardware configuration of the CIO-DAS1600 board if you do not have immediate access to ***Insta*Cal™** and/or your computer.

3.1 BASE ADDRESS

Unless there is already a board in your system using address 300 hex (768 decimal), leave the switches as they are set at the factory.

In Figure 3-1, the CIO-DAS1600 is set at base address 300 hex. This means the DAS-16 compatible section of the board is at 300 hex and the DIO-24 compatible section of the board is at 700 hex.

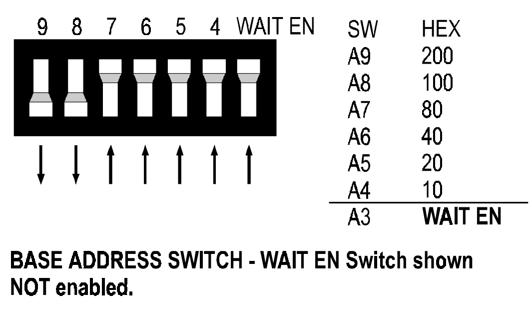

Figure 3-1. Base Address & Wait EN Switch

Note: Wait State Enable is typically not required. Leave the WAIT EN switch in the UP (not enabled) position

3.2 DMA LEVEL SELECT

If you are installing the board in an old XT bus computer, DMA level 3 is probably used by the hard disk controller. Set the DMA level switch to level 1 position (Figure 3-2).

If you have a 386 or higher computer, the hard disk controller does not use either DMA level 1 or 3 so either level can be selected. The default level is level 1.

Figure 3-2. DMA Level Select Switch

There are other boards that use DMA levels. Some network boards do and so do some IEEE-488 interface boards. Check to see if you have other boards in your computer that use DMA channels 1 or 3.

3.3 1/10 MHz XTAL JUMPER

The 1/10 MHz XTAL jumper selects the frequency of the square wave used as a clock by the A/D pacer circuitry. This pacer circuitry controls the sample timing of the A/D. The output driving the A/D converter is also available at the CTR 2 output pin on the main connector.

To maintain full compatibility with the original DAS-16, the CIO-DAS1600 required a 1 MHz crystal oscillator. When the DAS-16 was redesigned, a faster 10MHz crystal was added. A jumper is provided to maintain compatibility with older software. The CIO-DAS1600 has the jumper because the DAS-16 has the jumper and some existing software requires the jumper to be in the 1 MHz position while other software requires a 10 MHz oscillator. The CIO-DAS1600 is shipped with the jumper in the 1 MHz position (Figure 3-3).

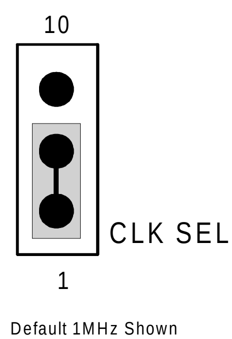

Figure 3-3. 1 or 10 MHz Select Jumper

3.4 8/16 CHANNEL SELECT

The analog inputs of the CIO-DAS1600 can be configured as eight differential or 16 single-ended. Use the single-ended input mode if you have more than eight analog inputs to sample. Using the differential input mode allows up to 10 volts of common mode (ground loop) rejection and will provide better noise immunity.

The CIO-DAS1600 comes from the factory configured for 16 single-ended inputs and the 8/16 switch is in the position shown in Figure 3-4. Set it for the type and number of inputs you desire. This switch is located under the metal shield. If you need access to this switch, this shield may be removed by removing the two screws on the back of the CIO-DAS1600.

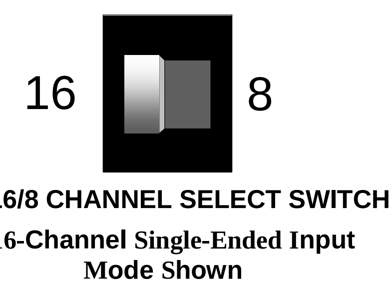

Figure 3-4. 8/16 Channel Select Switch

3.5 D/A CONVERTER REFERENCE JUMPER BLOCK

The jumper block located near the center of the CIO-DAS1600 allows you to use the on board precision voltage reference to select the output ranges of the digital to analog converters.

Analog output is provided by two 12-bit multiplying D/A converters. This type of converter accepts a reference voltage and provides an output proportional to that. The proportion is controlled by the D/A output code (0 to 4095). Each bit represents 1/4096 of full scale.

A precision −5V and −10V reference provide onboard D/A ranges of 0 to 5V, 0 to 10V, ±5V, ±10V. Other ranges between 0V and 10V are available if you provide a precision voltage reference at pin 10 or 26 of the main connector.

When the DAC0 reference is supplied onboard, pin 26 of the 37 pin connector is unused and can be employed as a simultaneous sample & hold trigger for use with the CIO-SSH16. To do so, place the jumper between the two pins SH (Figure 3-5).

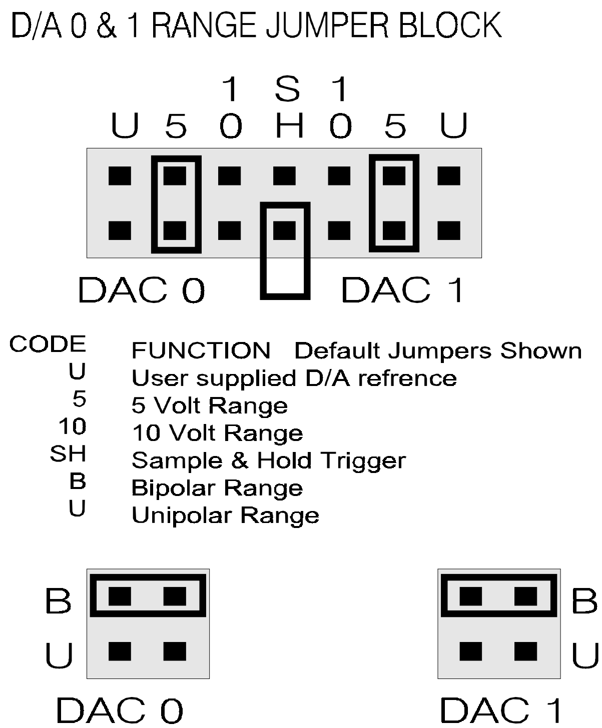

Figure 3-5. D/A Output Range Jumper Block

3.6 BIPOLAR/UNIPOLAR AND GAIN SETTING

The Bipolar or Unipolar configuration of the A/D converter is set by a switch (Figure 3-6). The switch controls all A/D channels. Though you cannot run some channels bipolar and some unipolar, you can measure a unipolar input in the bipolar mode. (e.g. you can monitor a 0 to 5V input with a ±5 V channel)

The input amplifier gain is controlled by a software programmed register located at BASE + B hex (11 decimal). The codes have different meaning for each board in the CIO-DAS1600 family. Refer to the Register Architecture section for details on this register.

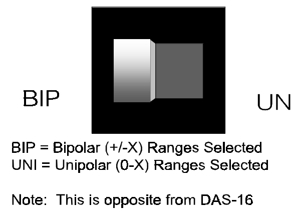

Figure 3-6. Bipolar/Unipolar Select Switch

3.7 PACER EDGE SELECT

The original Keithley MetraByte DAS-1600 was designed such that A/D conversion was initiated on the falling edge of the convert signal. Neither the original DAS-16, nor any of the other DAS-16 derivative converts on the falling edge. In fact, we are not aware of any A/D board that uses the falling edge to initiate the A/D conversion.

When using the falling edge to start the conversion, the A/D may be falsely triggered by 8254 pacer clock initialization glitching (easy to avoid but a real possibility in the DAS-1600). Converting on the falling edge mode also may lead to timing differences if the CIO-DAS1600 board is being used as a replacement for an older DAS16 series board.

Because using the falling edge trigger is undesirable, we have designed a jumper into the CIO-DAS1600 which allows you to choose which edge of the internal pacer signal starts the A/D conversion. The jumper has no effect on an external pacer signal (EXTCLOCK). The only reason we supply you the option of a falling edge trigger is to provide complete compatibility for those who have developed software for a DAS-1600 using the AS-1600 drivers, *AND,* when using the CIO-DAS1600 with that software you observe sample timing differences.

The CIO-DAS1600 is shipped with this jumper in the rising edge position. Figure 3-7 to the right shows the edge selection options. For compatibility with all third party packages, with all DAS-16 software and with CIO-DAS1600 software, leave this jumper in the rising edge position

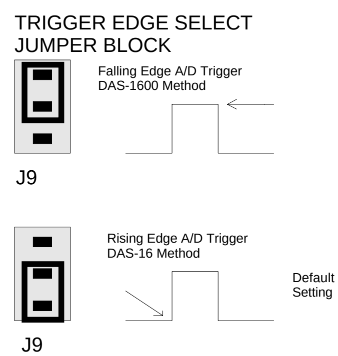

Figure 3-7. Trigger Edge Select Jumper

AUXILIARY TRIGGER

There is a position for a header connector at the rear of the CIO-DAS1600. This connector provides the same function as that found on the DAS-1600.

The A/D trigger signal can come from this connector, if installed. A jumper controls which pin the trigger signal comes in from. We do not install this connector (nor is it installed on the DAS-1600).

3.8 BURST MODE GENERATOR

The burst mode generator is a clock signal that paces the A/D at the maximum multi-channel sample rate, then periodically, performs additional maximum rate scans. In this way, the channel to channel skew (time between successive samples in a scan) is minimized without taking a large number of undesired samples (Figure 3-8).

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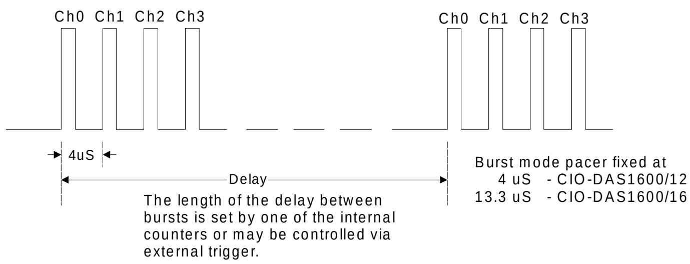


Figure 3-8. Burst Mode Timing

The CIO-DAS1600 burst mode generator takes advantage of the fast A/D. The burst mode skew is 4 µs between channels for the CIO-DAS160#/12. It is 13.3 µs for the CIO-DAS1602/16.

3.9 DT-CONNECT

There is no hardware configuration or installation required for DT-Connect. Software enables/disables DT-Connect, and of course, you must have a DT-Connect equipped accessory board, (Measurement Computing's MEGA-FIFO, for example) before using the DT-Connect.

DT-CONNECT IN MASTER MODE ONLY

The CIO-DAS1600 implements DT-Connect MASTER MODE only. DT-Connect is always enabled and is never busy. The ENABLED and BUSY signal levels are fixed in hardware. Since DT-Connect is always enabled, any A/D conversions are always transferred out through the DT-Connect port regardless of the bus transfer method specified. The CIO-DAS1600 can only operate in DT-Connect schemes where it is the sole master.

To assure that DT-Connect is properly initialized prior to any A/D transfer, the DT-Connect DT-Request handshake line is reset each time the programmable gain (Base + 11 decimal) register is written to. Therefore, it is not possible to use the DT-Connect for A/D sets which involve setting the gain between samples. This is not really a problem because any such scheme would be low speed and therefore store data to disk, obviating the need to use DT-Connect to store data on the MEGA-FIFO.

Please see the data sheet on the MEGA-FIFO, a 128 million-sample buffer board as an example of a DT-Connect accessory.

4 CONNECTOR PINOUTS

4.1 MAIN CONNECTOR DIAGRAM

The CIO-DAS1600 analog connector is a 37-pin "D" connector accessible from the rear of the PC through the expansion back plate. An additional signal, SS&H OUT, is available at pin 26. It is required when the CIO-SSH16 Simultaneous Sample and Hold card is used with a CIO-DAS1600 (Figure 4-1).

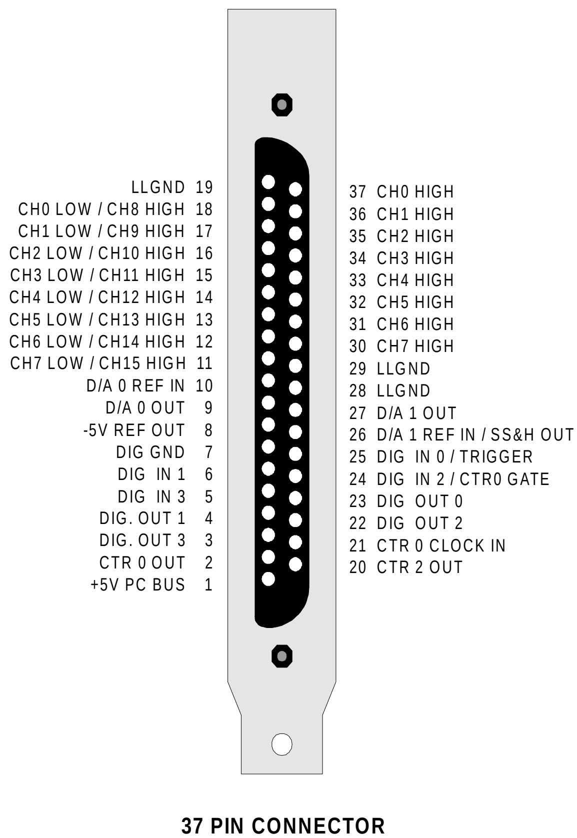
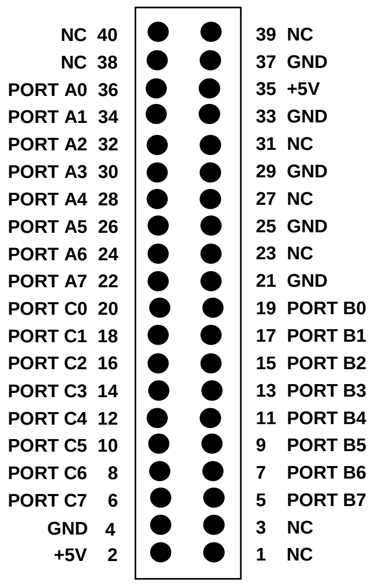


Figure 4-1. Main Analog Connector Pinout

The connector accepts female 37-pin D-type connectors, such as those on the C73FF-2, two foot cable with connectors. If frequent changes to signal connections or signal conditioning is required we strongly recommend purchasing the CIO-MINI37 screw terminal board and the mating C37FF-2 cable

4.2 DIGITAL I/O CONNECTOR (NOT APPLICABLE TO -P5 VERSIONS)

The digital I/O connector is mounted at the rear of the CIO-DAS1600 and will accept a 40-pin header connector. The optional BP40-37 cable assembly brings the signals to a back plate with a 37-pin male connector mounted in it. When connected through the BP40-37, the CIO-DAS1600 digital connector is identical to the CIO-DIO24 connector. The pin out of the 40- pin digital connector and the BP40-37 cable assembly are shown in Figure 4-2 below.



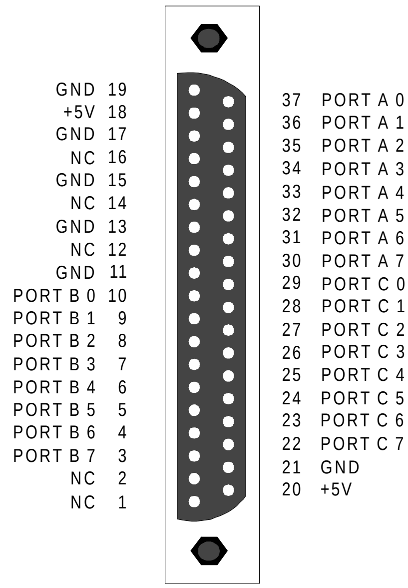


Figure 4-2. Digital 40-Pin Connector Pinout - BP40-37 Cable Assembly to Back Panel Pinout

5 ANALOG CONNECTIONS

5.1 ANALOG INPUTS

Analog signal connection is one of the most challenging aspects of applying a data acquisition board. If you are an Analog Electrical Engineer then this section is not for you, but if you are like most PC data acquisition users, the best way to connect your analog inputs may not be obvious. Though complete coverage of this topic is well beyond the scope of this manual, the following section provides some explanations and helpful hints regarding these analog input connections. This section is designed to help you achieve the optimum performance from your CIO-DAS1600 series board.

Prior to jumping into actual connection schemes, you should have at least a basic understanding of Single-Ended/Differential inputs and system grounding/isolation. If you are already comfortable with these concepts you may wish to skip to the next section (on wiring configurations).

5.1.1 Single-Ended and Differential Inputs

The CIO-DAS1600 provides either eight differential or 16 single-ended input channels.

Single-Ended Inputs

A single-ended input measures the voltage between the input signal and ground. In this case, in single-ended mode the CIO-DAS1600 measures the voltage between the input channel and LLGND. The single-ended input configuration requires only one physical connection (wire) per channel and allows the CIO-DAS1600 to monitor more channels than the (2-wire) differential configuration using the same connector and onboard multiplexor. However, since the CIO-DAS1600 is measuring the input voltage relative to its own low level ground, single-ended inputs are more susceptible to both EMI (Electro-Magnetic Interference) and any ground noise at the signal source. Figure 5-1a and 5-1b show the theory of single-ended input configuration

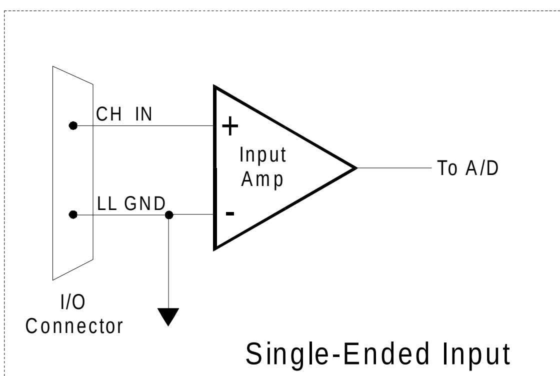


Figure 5-1a. Single-Ended Voltage Input Theory

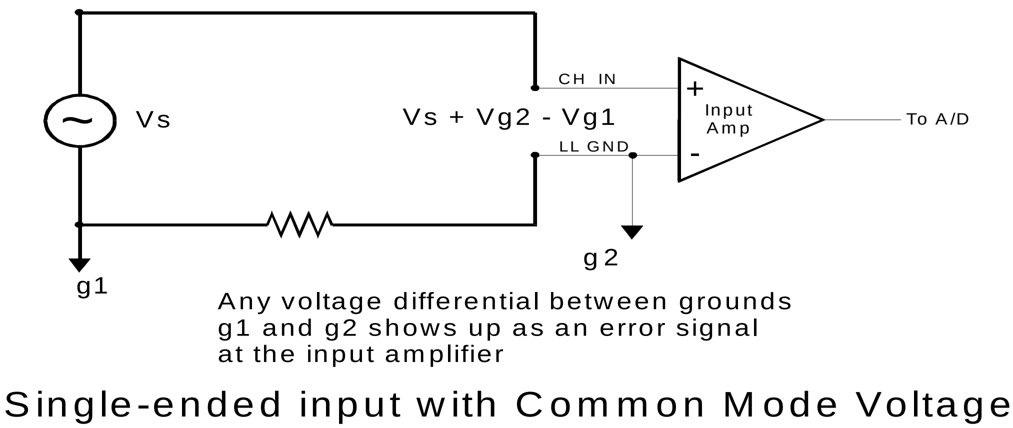


Figure 5-1b. Single-Ended Voltage Input Theory

Differential Inputs

Differential inputs measure the voltage between two distinct input signals. Within a certain range (referred to as the common mode range), the measurement is almost independent of signal source to CIO-DAS1600 ground variations. A differential input is also much more immune to EMI than a single-ended one. Most EMI noise induced in one lead is also induced in the other, the input only measures the difference between the two leads, and the EMI common to both is ignored. This effect is a major reason there is twisted pair wire as the twisting assures that both wires are subject to virtually identical external influence. Figure 5-2a and 5-2b below show a typical differential input configuration.

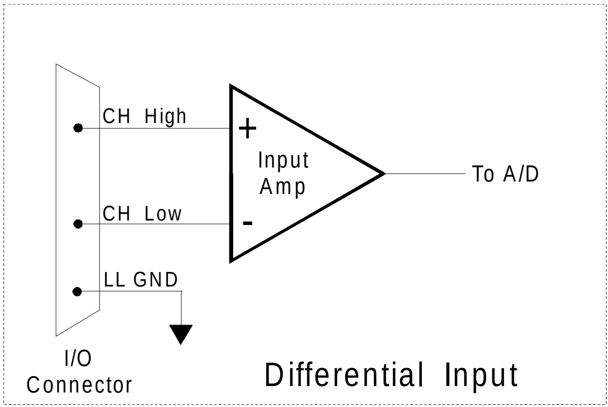


Figure 5-2a . Differential Input Theory

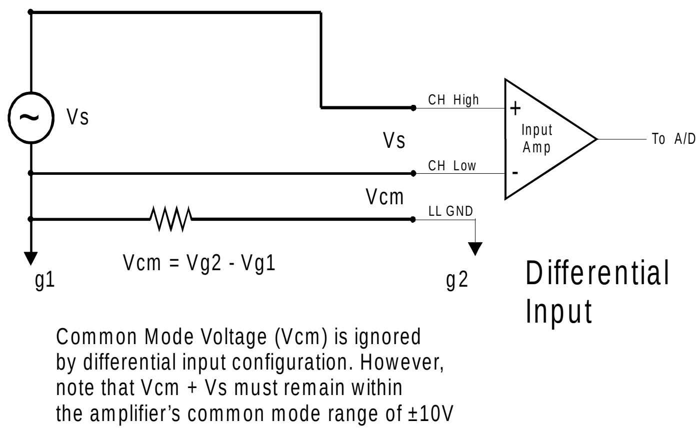


Figure 5-2b. Differential Input Theory

Before moving on to the discussion of grounding and isolation, it is important to explain the concepts of common mode, and common mode range (CM Range). Common mode voltage is depicted in the diagram above as Vcm. Though differential inputs measure the voltage between two signals, without (almost) respect to the either signal's voltages relative to ground, there is a limit to how far away from ground either signal can go. Though the CIO-DAS1600 has differential inputs, it will not measure the difference between 100V and 101V as 1 Volt (in fact the 100V would destroy the board!). This limitation or common mode range is depicted graphically in Figure 5-3. The CIO-DAS1600 common mode range is +/- 10 Volts. Even in differential mode, no input signal can be measured if it is more than 10V from the board's low level ground (LLGND).

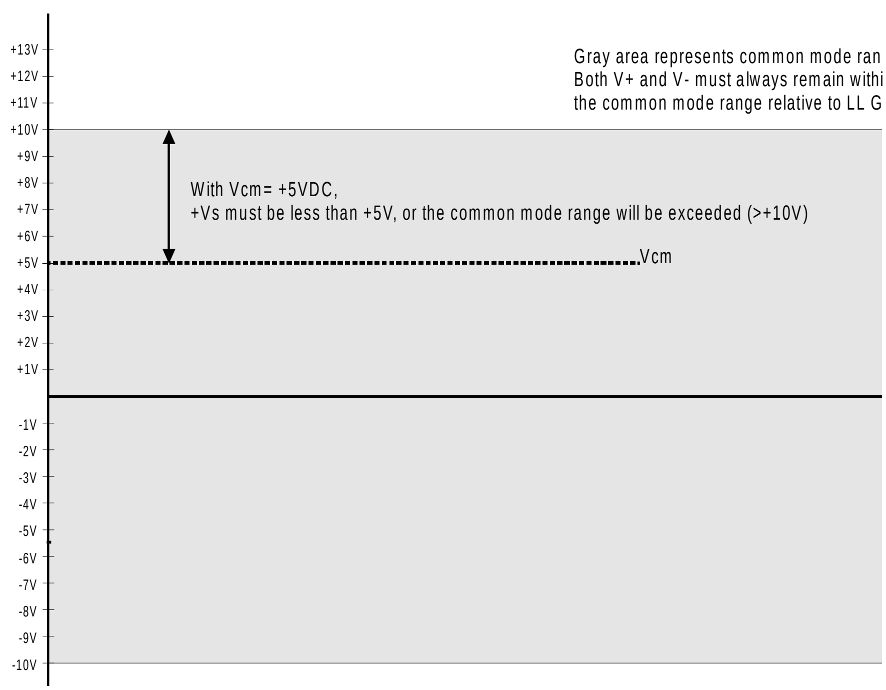


Figure 5-3. Common Mode Range

5.1.2 System Grounds and Isolation

There are three scenarios possible when connecting your signal source to your CIO-DAS1600 board.

1. The CIO-DAS1600 and the signal source have the same (or **common**) ground. This signal source can be connected directly to the CIO-DAS1600.

2. The CIO-DAS1600 and the signal source have an offset voltage between their grounds (AC and/or DC). This offset it commonly referred to a **common mode voltage**. Depending on the magnitude of this voltage, it may or may not be possible to connect the CIO-DAS1600 directly to your signal source. We will discuss this topic further in a later section.

3. The CIO-DAS1600 and the signal source already have **isolated grounds**. This signal source can be connected directly to the CIO-DAS1600.

Which system do you have?
Try the following experiment. Using a battery powered voltmeter*, measure the voltage (difference) between the ground signal at your signal source and at your PC. Place one voltmeter probe on the PC ground and the other on the signal source ground. Measure both the AC and DC Voltages.

**If you do not have access to a voltmeter, skip the experiment and take a look a the following three sections. You may be able to identify your system type from the descriptions provided.*

If both AC and DC readings are 0.00 volts, you may have a system with common grounds. However, since voltmeters will average out high frequency signals, there is no guarantee. Please refer to the section below titled ***Common Grounds***.

If you measure reasonably stable AC and DC voltages, your system has an offset voltage between the grounds category. This offset is referred to as a Common Mode Voltage. Please be careful to read the following warning and then proceed to the section describing ***Common Mode*** systems.

WARNING

If either the AC or DC voltage is greater than 10 volts, do not connect the CIO-DAS1600 to this signal source. You are beyond the boards usable common mode range and will need to either adjust your grounding system or add special Isolation signal conditioning to take useful measurements. A ground offset voltage of more than 30 volts will likely damage the CIO-DAS1600 board and possibly your computer. Note that an offset voltage much greater than 30 volts will not only damage your electronics, but it can also be hazardous to your health.

This is such an important point, that we will state it again. If the voltage between the ground of your signal source and your PC is greater than 10 volts, your board will not take useful measurements. If this voltage is greater than 30 volts, it will likely cause damage, and can represent a serious shock hazard! In this case you will need to either reconfigure your system to reduce the ground differentials, or purchase and install special electrical isolation signal conditioning.

If you cannot obtain a reasonably stable DC voltage measurement between the grounds, or the voltage drifts around considerably, the two grounds are most likely isolated. The easiest way to check for isolation is to change your voltmeter to it's ohm scale and measure the resistance between the two grounds. It is recommended that you turn both systems off prior to taking this resistance measurement. If the measured resistance is more than 100 Kohm, it's a fairly safe bet that your system has electrically ***isolated grounds***.

Systems with Common Grounds

In the simplest (but perhaps least likely) case, your signal source will have the same ground as the CIO-DAS1600. This would typically occur when providing power or excitation to your signal source directly from the CIO-DAS1600. There may be other common ground configurations, but it is important to note that any voltage between the CIO-DAS1600 ground and your signal ground is a potential error voltage if you set up your system based on a common ground assumption.

As a safe rule of thumb, if your signal source or sensor is not connected directly to an LLGND pin on your CIO-DAS1600, it's best to assume that you do not have a common ground even if your voltmeter measured 0.0 Volts. Configure your system as if there is ground offset voltage between the source and the CIO-DAS1600. This is especially true if you are using either the CIO-DAS1600/16 or the CIO-DAS1600/12 at high gains, since ground potentials in the sub-millivolt range will be large enough to cause A/D errors, yet will not likely be measured by your hand-held voltmeter.

***S*ystems with Common Mode (ground offset) Voltages**

The most frequently encountered grounding scenario involves grounds that are somehow connected, but have AC and/or DC offset voltages between the CIO-DAS1600 and signal source grounds. This offset voltage may be AC, DC or both and can be caused by a wide array of phenomena including EMI pickup, resistive voltage drops in ground wiring and connections, etc. Ground offset voltage is a more appropriate term to describe this type of system, but since our goal is to keep things simple, and help you make appropriate connections, we'll stick with our somewhat loose usage of the phrase Common Mode.

Small Common Mode Voltages

If the voltage between the signal source ground and CIO-DAS1600 ground is small, the combination of the ground voltage and input signal will not exceed the 'CIO-DAS1600's +/-10V common mode range, *(i.e. the voltage between grounds, added to the maximum input voltage, stays within +/-10V)*, This input is compatible with the CIO-DAS1600 and the system can be connected without additional signal conditioning. Fortunately, most systems will fall in this category and have a small voltage differential between grounds.

Large Common Mode Voltages

If the ground differential is large enough, the 'CIO-DAS1600's +/- 10V common mode range will be exceeded (i.e. the voltage between CIO-DAS1600 and signal source grounds, added to the maximum input voltage you're trying to measure exceeds +/-10V). In this case the CIO-DAS1600 cannot be directly connected to the signal source. You will need to change your system grounding configuration or add isolation signal conditioning. (Please look at our ISO-RACK and ISO-5B-series products to add electrical isolation, or give our technical support group a call to discuss other options.)

NOTE

Relying on the earth prong of a 120VAC for signal ground connections is not advised.. Different ground plugs may have large and potentially even dangerous voltage differentials. Remember that the ground pins on 120VAC outlets on different sides of the room may only be connected in the basement. This leaves the possibility that the "ground" pins may have a significant voltage differential (especially if the two 120VAC outlets happen to be on different phases.)

CIO-DAS1600 and signal source already have isolated grounds

Some signal sources will already be electrically isolated from the CIO-DAS1600. The diagram below shows a typical isolated ground system. These signal sources are often battery powered, or are fairly expensive pieces of equipment (since isolation is not an inexpensive proposition), isolated ground systems provide excellent performance, but require some extra effort during connections to assure optimum performance is obtained. Please refer to the following sections for further details.

5.2 Wiring Configurations

Combining all the grounding and input type possibilities provides us with the following potential connection configurations. The combinations along with our recommendations on usage are shown in Table 5-1 below.

Table 5-1. Input vs. Grounding Recommendations

Ground Category	Input Configuration	Our Recommendation
Common Ground	Single-Ended Inputs	Recommended
Common Ground	Differential Inputs	Acceptable
Common Mode Voltage < +/-10V	Single-Ended Inputs	Not Recommended
Common Mode Voltage < +/-10V	Differential Inputs	Recommended
Common Mode Voltage > +/- 10V	Single-Ended Inputs	Unacceptable without adding Isolation
Common Mode Voltage > +/-10V	Differential Inputs	Unacceptable without adding Isolation
Already Isolated Grounds	Single-ended Inputs	Acceptable
Already Isolated Grounds	Differential Inputs	Recommended

The following sections depicts recommended input wiring schemes for each of the eight possible input configuration/grounding combinations.

5.2.1 Common Ground / Single-Ended Inputs

Single-ended is the recommended configuration for common ground connections. However, if some of your inputs are common ground and some are not, we recommend you use the differential mode. There is no performance penalty (other than loss of channels) for using a differential input to measure a common ground signal source. However the reverse is not true. Figure 5-4 below shows a recommended connection diagram for a common ground / single-ended input system

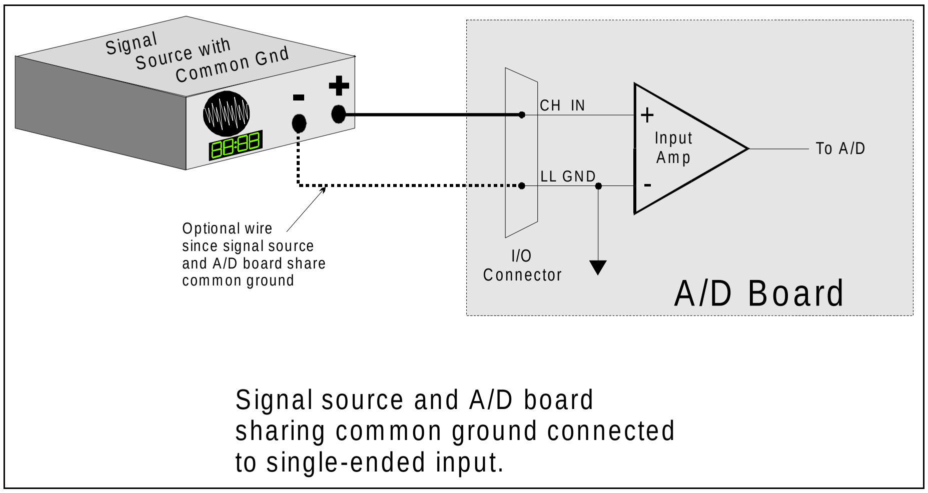


Figure 5-4. Common Ground / Single-Ended Inputs

5.2.2 Common Ground / Differential Inputs

The use of differential inputs to monitor a signal source with a common ground is a acceptable configuration though it requires more wiring and offers fewer channels than selecting a single-ended configuration. Figure 5-5 below shows the recommended connections in this configuration.

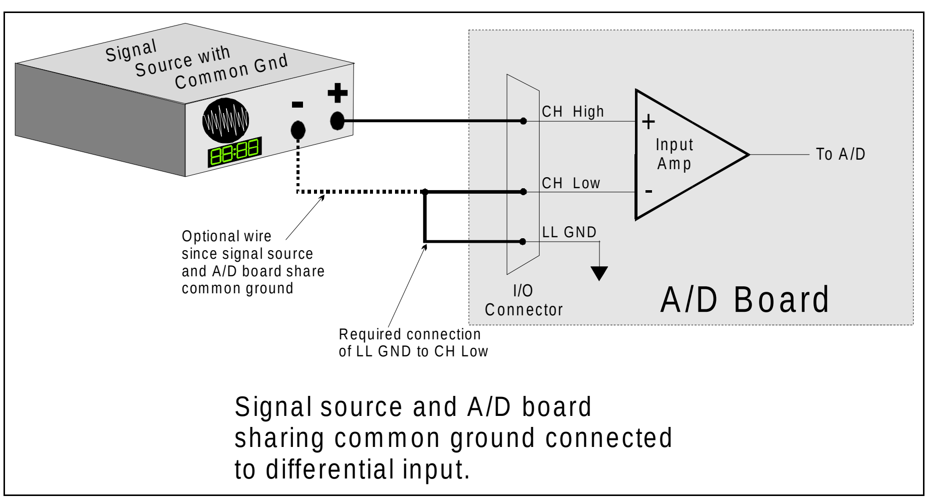


Figure 5-5. Common Ground / Differential Inputs

5.2.3 Common Mode Voltage < +/-10V / Single-Ended Inputs

This is not a recommended configuration. In fact, the phrase common mode has no meaning in a single-ended system and this case would be better described as a system with offset grounds. You can try this configuration, no system damage should occur and you may receive acceptable results.

5.2.4 Common Mode Voltage < +/-10V / Differential Inputs

Systems with varying ground potentials should always be monitored in the differential mode. Care is required to assure that the sum of the input signal and the ground differential (referred to as the common mode voltage) does not exceed the common mode range of the A/D board (±10V on the CIO-DAS1600). Figure 5-6 below show recommended connections in this configuration.

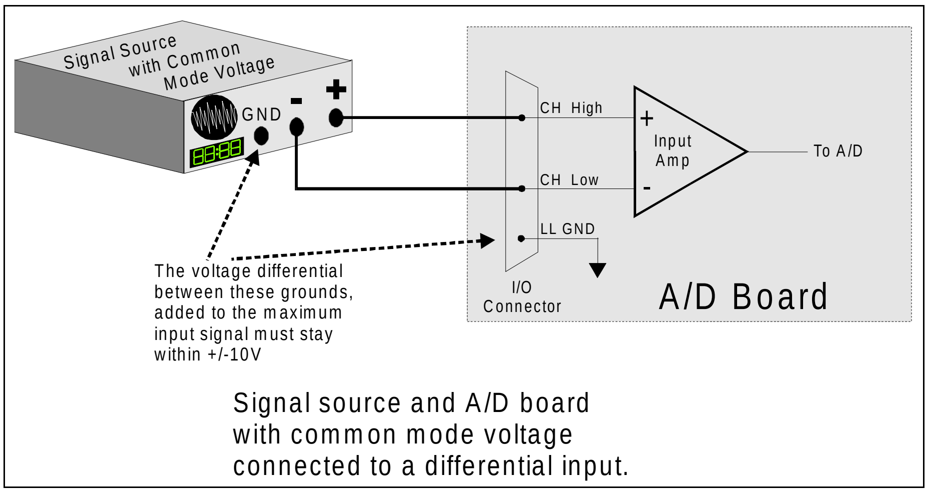


Figure 5-6. Common Mode Voltage < +/-10V / Differential Inputs

5.2.5 Common Mode Voltage > +/-10V

The CIO-DAS1600 will not directly monitor signals with common mode voltages greater than +/-10V. You will either need to alter the system ground configuration to reduce the overall common mode voltage, or add isolated signal conditioning between the source and your board. See Figure 5-7 and 5-8 below.

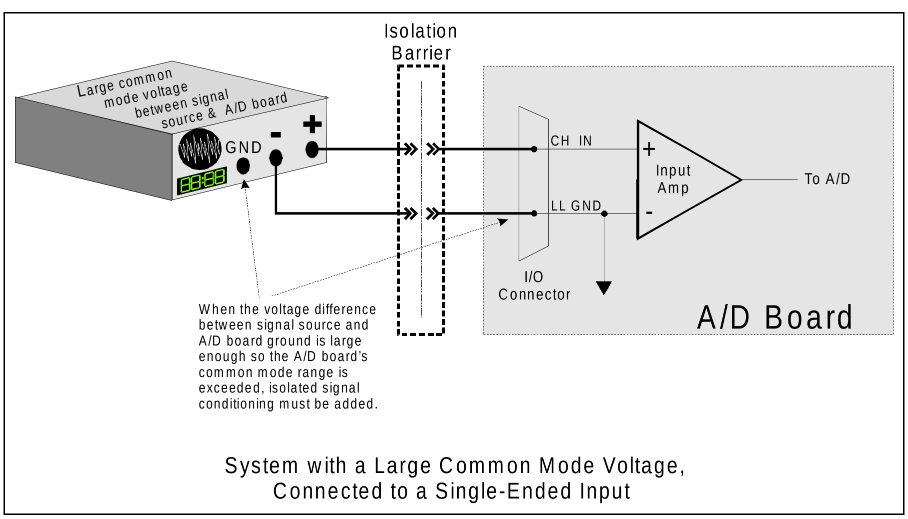


Figure 5-7. Common Mode Voltage > +/-10V. Single-Ended Input

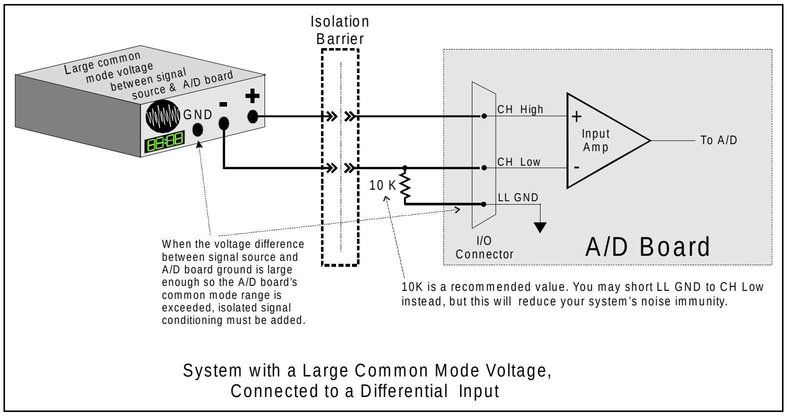


Figure 5-8. Common Mode Voltage > +/-10V. Differential Input

5.2.6 Isolated Grounds / Single-Ended Inputs

Single-ended inputs can be used to monitor isolated inputs, though the use of the differential mode will increase you system's noise immunity. Figure 5-9 below shows the recommended connections is this configuration.

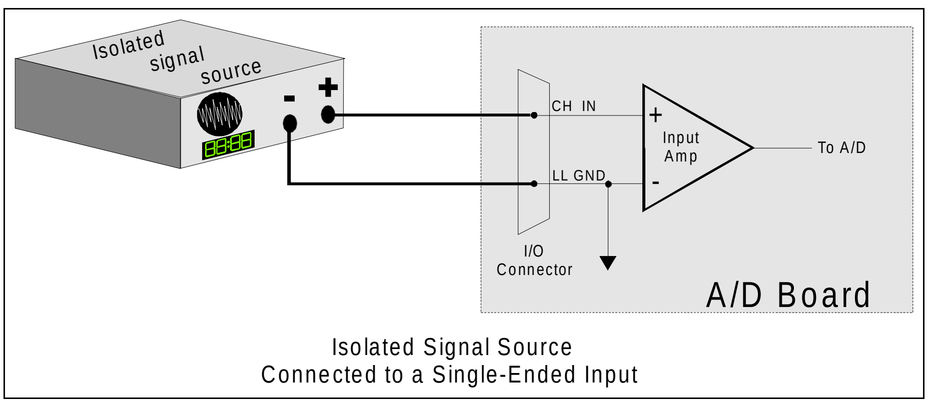


Figure 5-9. Isolated Grounds / Single-Ended Input

5.2.7 Isolated Grounds / Differential Inputs

Optimum performance with isolated signal sources is assured with the use of the differential input setting. Figure 5-10 below shows the recommend connections is this configuration.

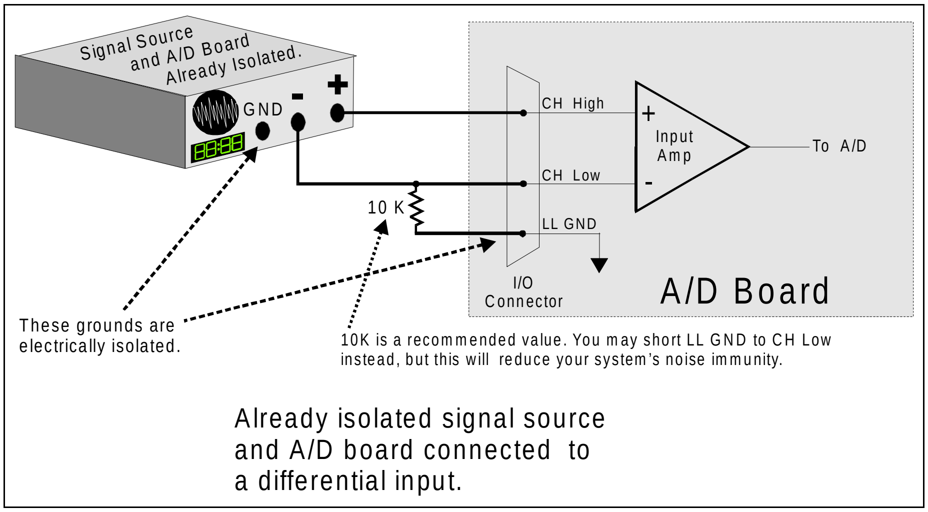


Figure 5-10. Isolated Grounds / Differential Inputs

5.3 ANALOG OUTPUTS

Analog outputs are simple voltage outputs which can be connected to any device which will record, display or be controlled by a voltage. The CIO-DAS1600 analog outputs are 4 quadrant multiplying DACs. This means that they accept an input voltage reference and provide an output voltage which is inverse to the reference voltage and proportional to the digital value in the output register.

For example, in unipolar mode, the supplied reference of −5V provides a +5V output when the value in the output register is 4095 (full scale at 12 bits of resolution). It provides a value of 2.5V when the value in the output register is 2048.
Figure 5-11 shows the onboard reference internally jumpered. Both D/A outputs will have a range of −5 to +5 volts. This is the default factory configuration.

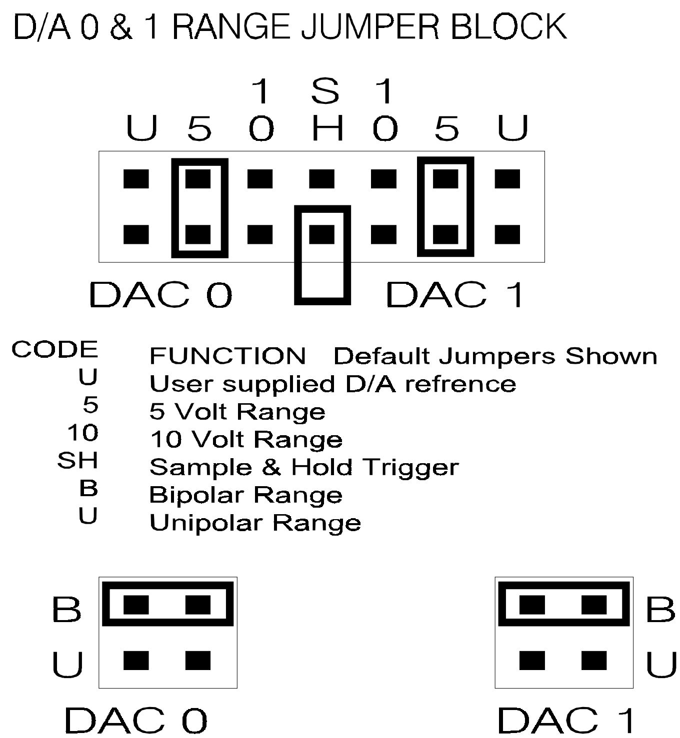


Figure 5-11. Analog Output Range Select Jumper Block

6 REGISTER ARCHITECTURE

There are three common approaches to generating software for the CIO-DAS1600. These are:

1. Writing custom software utilizing our Universal Library package
2. Using a fully integrated software package (e.g. Softwire)
3. Direct register level programming.

CUSTOM SOFTWARE UTILIZING THE UNIVERSAL LIBRARY
Most users write custom software using our Universal Library. The Universal Library takes care of all the board I/O commands and lets you concentrate on the application part of the software. For additional information regarding using the Universal Library, please refer to the documentation supplied with the Universal Library

FULLY INTEGRATED SOFTWARE PACKAGES (e.g. Softwire)
Many users also take advantage of the power and simplicity offered by one of the upper level data acquisition packages. Please refer to the package's documentation for setup and usage details.

DIRECT REGISTER LEVEL PROGRAMMING
Although uncommon, some applications do not allow the use of our Universal Library, and are not a good match for an upper level package. For these situations, detailed register mapping follows. This chapter is intended for experienced programmers only.

6.1 CONTROL & DATA REGISTERS

The CIO-DAS1600 is controlled and monitored by writing to and reading from 24 distinct I/O addresses. The first address is referred to as the BASE ADDRESS (BADR) and is set by a bank of switches on the board. All other addresses are located at the BASE ADDRESS plus a specified offset. In particular, the main analog I/O functions are controlled by the I/O addressees from BADR to BADR +15h and BADR +404h through BADR +407h. The additional 82C55 based digital I/O uses four consecutive I/O addresses at BASE ADDRESS + 400h (the -P5 versions do not include this 82C55).

Registers are easy to read from and write to, though to create a complete data acquisition software program at the register level is a significant undertaking. Unless there is a specific reason that you need to write your program at the register lever, we highly recommend the use of our Universal Library.

The method of programming required to set/read bits from bytes is beyond the scope of this manual. It will be covered in most Introduction To Programming books, available from a book store. The remainder of this chapter is included for those experienced programmers who wish to write their own register level programs.

In summary form, the registers and their functions are listed on Table 6-1 following. Within each register are eight bits which may constitute a byte of data or be eight individual bit set/read functions.

Table 6-1. Register Map

ADDRESS	READ FUNCTION	WRITE FUNCTION
BASE	A/D Data (Least significant)	Start A/D Conversion
BASE + 1	A/D Data (Most significant)	None
BASE + 2	Channel MUX	Channel MUX / FIFO reset
BASE + 3	Digital 4-Bit Input	Digital 4 Bit Output
BASE + 4	None	D/A 0 Least Significant bits
BASE + 5	None	D/A 0 Most Significant bits
BASE + 6	None	D/A 1 Least Significant bits
BASE + 7	None	D/A 1 Most Significant bits
BASE + 8	Status EOC, UNI/BIP etc.	Clear Interrupt
BASE + 9	DMA, Interrupt & Trigger Control	Set DMA, INT etc
BASE + Ah	none	Burst Length/pacer clk cntrl
BASE + Bh	PGA gain	PGA Control/DT reset
BASE + Ch	Counter 0 Data	Counter 0 Data
BASE + Dh	CTR 1 Data - A/D Pacer Clock	CTR 1 Data - A/D Pacer
BASE + Eh	CTR 2 Data - A/D Pacer Clock	CTR 2 Data - A/D Pacer
BASE + Fh	None. No read back on 8254	Pacer Clock Control (8254)
BASE + 400h	Port A Input of 8255	Port A Output, n/a on -P5 ver.
BASE + 401h	Port B Input	Port B Output, n/a on -P5 ver.
BASE + 402h	Port C Input	Port C Output, n/a on -P5 ver.
BASE + 403h	None. No read back on 8255	Configure 8255, n/a on -P5 ver.
BASE + 404h	None	Conversion Enable/Disable
BASE + 405h	None	Burst Mode Enable/Disable
BASE + 406h	None	DAS 1600 Enable/Disable
BASE + 407h	Status of extended features	None

6.1.1 A/D DATA & CHANNEL REGISTERS (CIO-DAS1600/12)

BASE ADDRESS +0

7	6	5	4	3	2	1	0
A/D 3	A/D 2	A/D 1	A/D 0 LSB	CH3	CH2	CH1	CH0

A read/write register.

READ
On read, it contains two types of data. The least significant four digits of the analog input data and the channel number from which the current data was taken.

These four bits of analog input data must be combined with the eight bits of analog input data in BASE + 1 to form a complete 12-bit number. The data format is 0 = –FS; 4095 = +FS.

The channel number is binary. If the current channel is 5, bits CH2 and CH0 are high, CH3 and CH1 are low.

WRITE
Writing any data to the register causes an immediate A/D conversion.

BASE ADDRESS +1

7	6	5	4	3	2	1	0
A/D 11 MSB	A/D 10	A/D 9	A/D 8	A/D 7	A/D 6	A/D 5	A/D 4

A Read-only register.

On read the most significant A/D byte is read.

6.1.2 A/D DATA & CHANNEL REGISTERS (CIO-DAS1602/16)

BASE ADDRESS

7	6	5	4	3	2	1	0
A/D 7	A/D 6	A/D 5	A/D 4	A/D 3	A/D 2	A/D 1	A/D 0 LSB

A read/write register.

READ
On read, it contains the least significant eight digits of the analog input data.

These eight bits of analog input data must be combined with the eight bits of analog input data in BASE + 1, to form a complete 16-bit number. The data format is 0 = –FS; 65,535 = +FS.

WRITE
Writing any data to the register causes an immediate A/D conversion.

BASE ADDRESS +1

7	6	5	4	3	2	1	0
A/D 15 MSB	A/D 14	A/D 13	A/D 12	A/D 11	A/D 10	A/D 9	A/D 8

A Read-only register.

On read the most significant A/D byte is read.

6.1.3 CHANNEL MUX SCAN LIMITS REGISTER

BASE ADDRESS +2

7	6	5	4	3	2	1	0
CH H3	CH H2	CH H1	CH H0	CH L3	CH L2	CH L1	CH L0

A read and write register.

READ
The current channel scan limits are read as one byte. The high channel number scan limit is in the most significant four bits. The low channel scan limit is in the least significant four bits.

WRITE
The channel scan limits desired are written as one byte. The high channel number scan limit is in the most significant four bits. The low channel scan limit is in the least significant four bits.

NOTE

Every write to this register sets the current A/D channel MUX setting to the number in bits 0-3 and resets the FIFO. See BASE + 8.

6.1.4 FOUR BIT DIGITAL I/O REGISTERS

BASE ADDRESS+3
A read and write register.

When read from...

7	6	5	4	3	2	1	0
1	1	0	0	DI3	DI2, CTR0, GATE	DI1	DI0, TRIG

READ
The signals present at the inputs are read as one byte, the most significant four bits of which are always zero. The pins 25 (digital input 0) and 24 (digital input 2) digital inputs have two functions each.

The TRIG function of digital input 0 can be used to hold off the first sample of an A/D set by holding it low (0V) until you are ready to take samples, which are then paced by the 8254. It can also be used as the source of an external start conversion pulse, synchronizing A/D conversions to some external event.

When written to..

7	6	5	4	3	2	1	0
X	X	X	X	DO3	DO2	DO1	DO0

WRITE
The upper four bits are ignored. The lower four bits are latched TTL outputs. Once written, the state of the inputs cannot be read back because a read back would read the separate digital input lines (see above).

NOTE

Since the digital inputs have multiple functions, use the digital input lines 0-3 with care when you are also using the A/D converter.

The digital outputs are also used by the CIO-EXP32, 32-channel analog multiplexer/amplifier.

6.1.5 D/A REGISTERS

D/A 0 REGISTERS

BASE ADDRESS +4

7	6	5	4	3	2	1	0
D/A3	D/A2	D/A1	D/A0 LSB	X	X	X	X

BASE ADDRESS + 5

7	6	5	4	3	2	1	0
D/A11 MSB	D/A10	D/A9	D/A8	D/A7	D/A6	D/A5	D/A4

D/A 1 REGISTERS

BASE ADDRESS + 6

7	6	5	4	3	2	1	0
D/A3	D/A2	D/A1	D/A0 LSB	X	X	X	X

BASE ADDRESS + 7

7	6	5	4	3	2	1	0
D/A11 MSB	D/A10	D/A9	D/A8	D/A7	D/A6	D/A5	D/A4

WRITE ONLY
Each 12 bit D/A output line has two registers. The first contains the four least significant bits of the data and four bits that don't care. The second register contains the eight most significant bits of the data.

The D/A will be updated when the eight most significant bits (upper register) are written. In this way, the lower four bits can be written with no effect on the D/A output until the remainder of the data is written to the upper eight bits.

6.1.6 STATUS REGISTER

BASE ADDRESS + 8

7	6	5	4	3	2	1	0
EOC	U/B	MUX	INT	CH3	CH2	CH1	CH0

A read mostly, one-function-write register.

READ

EOC = 1, the A/D converter is busy. EOC = 0, it is free.

U/B = 1, the amplifier is in Unipolar mode. U/B = 0, is bipolar.

MUX = 1, Channels are configured 16 single ended. MUX = 0, 8 differential.

INT = 1, an interrupt has been received. INT = 0, ready to receive an interrupt. An interrupt service routine must clear this bit after each interrupt.

CH3, CH2, CH1 & CH0 are a binary number between 0 and 15 indicating the MUX channel currently selected and is valid only when EOC = 0. The channel MUX increments shortly after EOC = 1 so may be in a state of transition when EOC = 1.

WRITE
A write of any data to this register sets the INT bit to 0.

6.1.7 DMA, INTERRUPT & TRIGGER CONTROL

BASE ADDRESS + 9

7	6	5	4	3	2	1	0
INTE	IR2	IR1	IR0	X	DMA	TS1	TS0

A read and write register.

READ
INTE = 1, Interrupts are enabled. An interrupt generated will be placed on the PC bus interrupt level selected by IR4, IR2 & IR1. INTE = 0, interrupts are disabled.

IR2, IR1, IR0 are bits in a binary number between 0 and 7 which map interrupts onto the PC bus interrupt levels 2 to 7. Interrupts 0 and 1 cannot be asserted by the CIO-DAS1600.

Table 6-2. Interrupt Program Codes

IR2	IR1	IR0	INTERRUPT LEVEL
0	0	0	None
0	0	1	None
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

When DMA = 1, DMA transfers are enabled.
When DMA = 0, DMA transfers are disabled.
Note that this bit only allows the CIO-DAS1600 to assert a DMA request to the PC on the DMA request level selected by the DMA switch on the CIO-DAS1600. Before this bit is set to 1, the PC's 8237 (or appropriate) DMA controller chip must be set up.

TS1 & TS0 control the source of the A/D start conversion trigger according to Table 6-3 below.

Table 6-3. Source Codes for the A/D Start Conversion Trigger

TS1	TS0	
0	X	Software triggered A/D only
1	0	Start on rising edge (Digital input 0, Pin 25)
1	1	Start on Pacer Clock Pulse (CTR 2 OUT, no external access)

6.1.8 PACER CLOCK CONTROL REGISTER

BASE ADDRESS + Ah

7	6	5	4	3	2	1	0
BL3	BL2	BL1	BL0	X	X	CTR0	TRIG0

Write only

BL3 to BL0 = BURST LENGTH. This nibble determines the number of conversions per trigger when in the burst mode. There are one to sixteen samples (single-ended) or eight samples (differential) in a burst. When the CIO-DAS1600 is not in the burst mode these bits have no function.

CTR0 = 1. When CTR0 = 1, an onboard 100 kHz clock signal is ANDed with the COUNTER 0 CLOCK INPUT (pin 21). A high on pin 21 will allow pulses from the onboard source into the 8254 Counter 0 input. (This input has a pull-up resistor on it, so no connection is necessary to use the onboard clock as a pacer clock.

CTR0 = 0. When CTR0 = 0, the input to 8254 Counter 0 is entirely dependent on pulses at pin 21, COUNTER 0 CLOCK INPUT.

TRIG0 = 1. When TRIG0 = 1 external gating of the pacer clock at pin 25 is enabled. Pin 25 going high will enable the pacer. The input at pin 25 is connected to a pull-up resistor and will remain high unless pulled low externally.

TRIG0 = 0. When TRIG0 = 0, the gating of the pacer clock at pin 25 is disabled. The gates of counter 1 & 2 are held high, preventing external control of the pacer gate.

Figure 6-1 may help you understand these registers. They are further explained in literature covering the 8254.

CIO-DAS1600 8254 PACER CLOCK & CONTROL

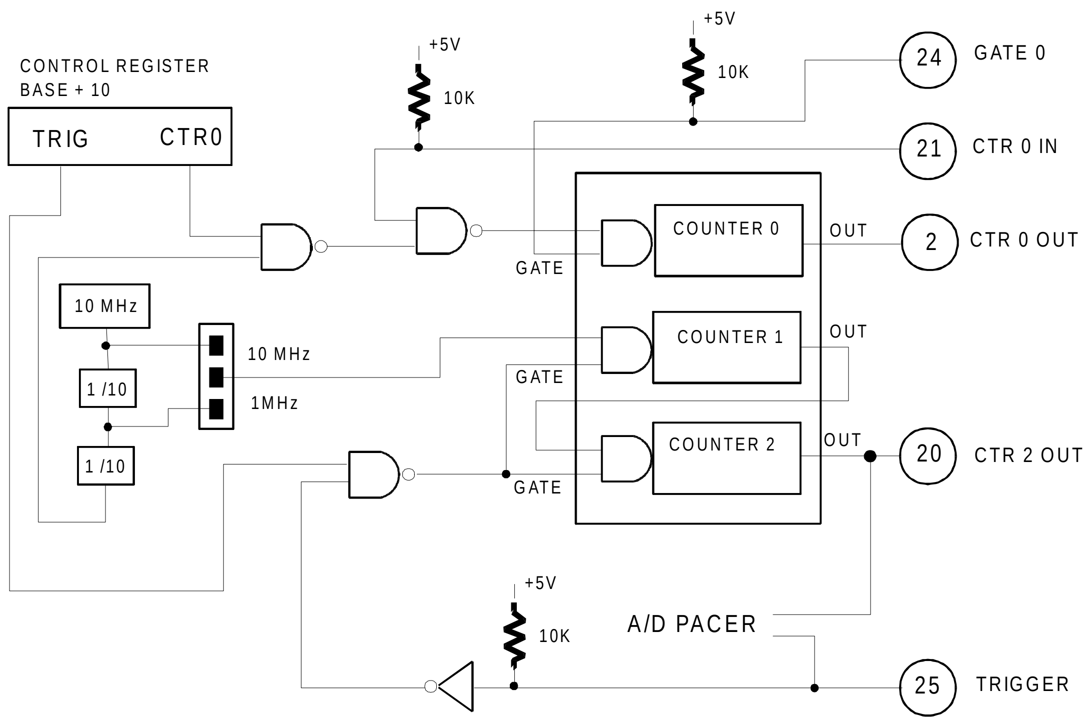


Figure 6-1. Pacer Clock Block Diagram

6.1.9 PROGRAMMABLE GAIN CONTROL REGISTER / BURST RATE

BASE ADDRESS + Bh

7	6	5	4	3	2	1	0
X	X	X	X	X	X	G1	G0

BURST RATE is fixed at: CIO-DAS1600/12 = 4 µs (250 kHz) between burst samples. CIO-DAS1602/16 = 13.3 µs between burst samples (75 kHz).

PROGRAMMABLE GAIN CONTROL: Range and gain is controlled by bits G1 and G0. The codes have different meaning for each board in the DAS1600 family (Table 6-4).

Table 6-4. Range Codes

BOARD	CODE	BIPOLAR RANGE	UNIPOLAR RANGE
CIO-DAS1601/12	0	+/-10V	0 to 10V
	1	+/-1V	0 to 1V
	2	+/-0.1V	0 to 0.1V
	3	+/-0.01V	0 to 0.01V
CIO-DAS1602/12 and CIO-DAS1602/16	0	+/-10V	0 to 10V
	1	+/-5V	0 to 5V
	2	+/-2.5V	0 to 2.5V
	3	+/-1.25V	0 to 1.25V

The range, unipolar or bipolar is controlled by a switch. If your application is better served by programmable ranges, please consider the CIO-DAS16/Jr or CIO-DAS16/330 boards.

DT-CONNECT NOTE:
To guarantee that DT-Connect is properly initialized prior to any A/D transfer, the DT-Connect DT-Request handshake line is reset each time this register is written to. Therefore, it is not possible to use the DT-Connect for A/D sets which involve setting the gain between samples. This is not really a problem because any such scheme would be low speed and therefore store data to disk, obviating the need to use DT-Connect to store data on the MEGA-FIFO.

6.1.10 PACER CLOCK DATA & CONTROL REGISTERS

8254 COUNTER 0 DATA
BASE ADDRESS + Ch

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

8254 COUNTER 1 DATA
BASE ADDRESS + Dh

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

8254 COUNTER 2 DATA
BASE ADDRESS + Eh

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

The three 8254 counter/timer data registers can be written to and read from. Because each counter will count as high as 64,535, it is clear that loading or reading the counter data must be a multi-step process. The operation of the 8254 is explained in Intel 8254 data sheet.

8254 COUNTER CONTROL
BASE ADDRESS + Fh

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

This register controls the operation and loading/reading of the counters. The configuration of the 82C54 codes which control the chip is explained in the Intel 82C54 data sheet.

6.1.11 24-bit DIGITAL I/O REGISTERS (not applicable on -P5 versions)

PORT A DATA
BASE ADDRESS + 400h

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

PORT B DATA
BASE ADDRESS +401h

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

Ports A & B can be programmed as input or output. Each is written to and read from in bytes, although for control and monitoring purposes the individual bits are used.

Bit set/reset and bit read functions require that unwanted bits be masked out of reads and ORed into writes.

PORT C DATA
BASE ADDRESS +402h

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0
CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

Port C can be used as one 8-bit port of either input or output, or it can be split into two 4-bit ports which can be independently input or output. The notation for the upper 4-bit port is CH3 - CH0, and for the lower, CL3 - CL0.

Although it can be split, every read and write to port C carries eight bits of data so unwanted information must be ANDed out of reads, and writes must be ORed with the current status of the other nibble.

OUTPUT PORTS
In 8255 mode 0 configuration, ports configured for output hold the output data written to them. This output byte can be read back by reading a port configured for output.

INPUT PORTS
In 8255 mode 0 configuration, ports configured for input read the state of the input lines at the moment. Transitions are not latched.

8255 CONTROL REGISTER
BASE ADDRESS +403h

7	6	5	4	3	2	1	0
MS	M3	M2	A	CU	M1	B	CL
	Group A				Group B		

The 8255 can be programmed to operate in Input/ Output (mode 0), Strobed Input/ Output (mode 1) or Bi-Directional Bus (mode 2).

When the PC is powered up or RESET, the 8255 is reset. This places all 24 lines in Input mode and no further programming is needed to use the 24 lines as TTL inputs.

To program the 8255 for other modes, the following control code byte must be assembled into an 8 bit byte.

MS = Mode Set. 1 = mode set active

M3	**M2**	**GROUP A FUNCTION**		
0	1	Mode 0	Input / Output	
0	1	Mode 1	Strobed Input / Output	
1	X	Mode 2	Bi-Directional Bus	
A	**B**	**CL**	**CH**	**INDEPENDENT FUNCTION**
1	1	1	1	Input
0	0	0	0	Output

M1 = 0 is mode 0 for group B.   Input / Output
M1 = 1 is mode 1 for group B.   Strobed Input / Output

The Ports A, B, C High and C Low can be independently programmed for input or output.

The two groups of ports, group A and group B, can be independently programmed in one of several modes. The most commonly used mode is mode 0, input / output mode. The codes for programming the 8255 in this mode are shown in Table 6-5 below.

Table 6-5. Programming Codes for the 82C55 Chip

D4	D3	D1	D0	HEX	DEC	A	CU	B	CL
0	0	0	0	80	128	OUT	OUT	OUT	OUT
0	0	0	1	81	129	OUT	OUT	OUT	IN
0	0	1	0	82	130	OUT	OUT	IN	OUT
0	0	1	1	83	131	OUT	OUT	IN	IN
0	1	0	0	88	136	OUT	IN	OUT	OUT
0	1	0	1	89	137	OUT	IN	OUT	IN
0	1	1	0	8A	138	OUT	IN	IN	OUT
0	1	1	1	8B	139	OUT	IN	IN	IN
1	0	0	0	90	144	IN	OUT	OUT	OUT
1	0	0	1	91	145	IN	OUT	OUT	IN
1	0	1	0	92	146	IN	OUT	IN	OUT
1	0	1	1	93	147	IN	OUT	IN	IN
1	1	0	0	98	152	IN	IN	OUT	OUT
1	1	0	1	99	153	IN	IN	OUT	IN
1	1	1	0	9A	154	IN	IN	IN	OUT
1	1	1	1	9B	155	IN	IN	IN	IN

NOTE: D7 is always 1; D6, D5, and D2 are always 0.

6.1.12 CONVERT DISABLE REGISTER

BASE ADDRESS + 404h

7	6	5	4	3	2	1	0
T	T	T	T	T	T	T	T

WRITE ONLY. Writing a 0 to this register enables triggering of the A/D converter if the DAS1600 mode is enabled. On power-up or reset this register is reset to conversion triggers enabled. Writing a 40 hex to this register disables A/D conversions.

6.1.13 BURST MODE ENABLE REGISTER

BASE ADDRESS + 405h

7	6	5	4	3	2	1	0
B	B	B	B	B	B	B	B

WRITE ONLY. Burst mode enable. Writing 40 hex to this register enables the burst trigger. Writing 0 to this register disables burst trigger. On power-up or reset the burst trigger is disabled.

6.1.14 DAS1600 MODE ENABLE REGISTER

BASE ADDRESS +406h

7	6	5	4	3	2	1	0
M	M	M	M	M	M	M	M

WRITE ONLY. DAS1600 mode enable. Writing 40 hex to this register enables the DAS1600 functions. Writing 0 to this register disables DAS1600 functions. On power-up or reset the DAS1600 functions are disabled.

6.1.15 BURST STATUS REGISTER

BASE ADDRESS + 407h

7	6	5	4	3	2	1	0
0	BME	ME	CD	0	0	WS	CLK

READ ONLY. This register provides status on:

a. The clock select switch and wait state switch.
b. The DAS1600 enable, Conversion Disable and Burst Mode Enable bits.

The register defaults to 000100XX on power-up or reset, which corresponds to the programmable bit default settings plus the state of the switches. The bit assignments are as follows.

BME 1 = Burst Mode Enabled, 0 = disabled.
ME 1 = DAS1600 Mode Enabled, 0 = disabled.
CD 1 = Conversions allowed, 0 = conversions disabled.
WS 1 = Wait State Enabled, 0 = No wait state.
CLK 1 = 10 MHz clock selected, 0 = 1 MHz clock selected.

7 CALIBRATION AND TEST

Every board was fully tested and calibrated at the factory. For normal environments, a calibration interval of six months to one year is recommended. If frequent variations in temperature or humidity are common, recalibrate at least once every three months. It requires less than 20 minutes to calibrate the CIO-DAS1600.

The A/D is calibrated by applying a known voltage to an analog input channel and adjusting trim pots for offset and gain. There are three trim pots requiring adjustment to calibrate the analog input section of the CIO-DAS1600. There are also three pots associated with each of the analog output channels. The entire procedure is described in detail in the ***Insta*****Cal**™, calibration routine.

The CIO-DAS1600 should be calibrated for the range you intend to use it in. When the range is changed, slight variation in zero and full scale may result. These variations can be measured and removed in software if necessary.

8 ANALOG ELECTRONICS

8.1 VOLTAGE DIVIDERS

If you wish to measure a signal which varies over a range greater than the input range of an analog or digital input, a voltage divider can drop the voltage of the input signal to the level the analog or digital input can measure.

A voltage divider applies Ohm's law, which states,
Voltage = Current * Resistance (V = I * R)
and Kirkoff's voltage law which states,

> The sum of the voltage drops around a circuit will be equal to the voltage drop for the entire circuit.

Implied in the above is that any variation in the voltage drop for the circuit as a whole will have a proportional variation in all the voltage drops in the circuit.

A voltage divider takes advantage of the fact that the voltage across one of the resistors in a circuit is proportional to the voltage across the total resistance in the circuit.

The object in using a voltage divider is to choose two resistors with the proper proportions relative to the full scale of the analog or digital input and the maximum signal voltage (Figure 8-1).

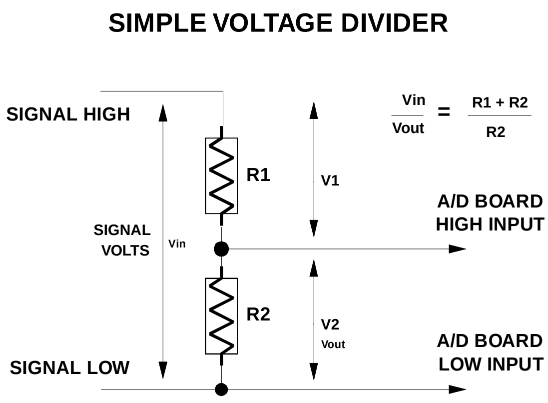


Figure 8-1. Voltage Divider Schematic

Reducing a voltage proportionally is called attenuation. The formula for attenuation is:

$$\text{Attenuation} = \frac{R1 + R2}{R2}$$

The variable Attenuation is the proportional difference between the signal voltage max and the full scale of the analog input.

$$2 = \frac{10K + 10K}{10K}$$

For example, if the signal varies between 0 and 20 volts and you wish to measure that with an analog input with a full scale range of 0 to 10 volts, the Attenuation is 2:1 or just 2.

$$R1 = (A - 1) * R2$$

For a given attenuation, pick a handy resistor and call it R2, then use this formula to calculate R1.

Digital inputs also make use of voltage dividers, for example, if you wish to measure a digital signal that is at 0 volts when off and 24 volts when on, you cannot connect that directly to the CIO-AD digital inputs. The voltage must be dropped to 5 volts max when on. The Attenuation is 24:5 or 4.8. Use the equation above to find an appropriate R1 if R2 is 1K. Remember that a TTL input is 'on' when the input voltage is greater than 2.5 volts.

IMPORTANT NOTE: The resistors, R1 and R2, are going to dissipate all the power in the divider circuit according to the equation Current = Voltage / Resistance. The higher the value of the resistance (R1 + R2) the less power dissipated by the divider circuit. Here is a simple rule:

For Attenuation of 5:1 or less, no resistor should be less than 10K.

For Attenuation of greater than 5:1, no resistor should be less than 1K.

The CIO-TERMINAL has the circuitry on board to create custom voltage dividers. The CIO-TERMINAL is a 16" by 4" screw terminal board with two 37 pin D type connectors and 56 screw terminals (12 - 22 AWG). Designed for table top, wall or rack mounting, the board provides prototype, divider circuit, filter circuit and pull-up resistor positions which you can complete with the proper value components for your application.

8.2 LOW PASS FILTERS

A low-pass filter is placed on the signal wires between a signal and an A/D board. It stops frequencies greater than the cut off frequency from entering the A/D board's analog or digital inputs.

The key term in a low-pass filter circuit is cutoff frequency. The cutoff frequency is that frequency above which no variation of voltage with respect to time can enter the circuit. For example, if a low-pass filter had a cutoff frequency of 30 Hz, the kind of interference associated with line voltage (60Hz) would be filtered out but a signal of 25 Hz would be allowed to pass.

Also, in a digital circuit, a low-pass filter might be used to “de-bounce” an input from a momentary contact switch or a relay closure.

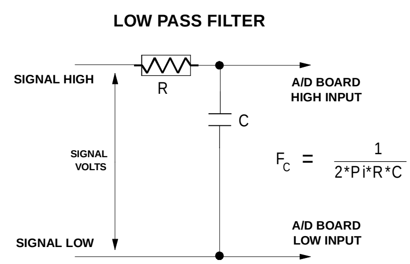


Figure 8-2. Low-Pass Filter Schematic

A simple low-pass filter (Figure 8-2) can be constructed from one resistor (R) and one capacitor (C). The cutoff frequency is determined according to the formula:

$$Fc = \frac{1}{2 * \pi * R * C}$$

$$R = \frac{1}{2 * \pi * C * Fc}$$

Where : π = 3.14....
R = ohms
C = farads

9 SPECIFICATIONS

9.1 CIO-DAS1601/12 & CIO-DAS1602/12

Power consumption	
+5	1.4 A typical, 2.1 A max
Analog input section	
A/D converter type	ADS7800 successive approximation
Resolution	12 bits
Programmable ranges	
CIO-DAS1601/12	±10V, ±1V, ±0.1V, ±0.01V, 0 to 10V, 0 to 1V, 0 to 0.1V, 0 to 0.01V
CIO-DAS1602/12	±10V, ±5V, ±2.5V, ±1.25V, 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V
A/D pacing	Programmable: external source (Din0, positive edge) or internal counter (positive or negative edge, jumper-select able) or software-polled
Burstmode	4 µs
Data transfer	From 512 sample FIFO via interrupt, DMA, DT-Connect to external memory board or software polled
Polarity	Unipolar/Bipolar, switch selectable
Number of channels	8 differential or 16 single-ended, switch selectable
Interrupts	2 to 7
Interrupt enable	Programmable
Interrupt sources	End-of-conversion, terminal count (DMA)
DMA	Channel 1 or 3
Trigger sources	External hardware/software (DIn0)
A/D conversion time	3.3 µs
Throughput	
DMA	160 kHz
DT-Connect (multi-channel)	250 kHz
DT-Connect (single-channel)	330 kHz
Differential Linearity error	±1 LSB
Integral Linearity error	±1 LSB
No missing codes guaranteed	12 bits
Gain drift	±60 ppm/°C
Zero drift	±160 ppm/°C
Input leakage current (@25 Deg C)	200 nA
Input impedance	Min 10 Megohms
Absolute maximum input voltage	±35V

Analog Output:

Resolution	12 bits
Number of channels	2
D/A type	MX7548
Voltage Ranges	±10V, ±5V, 0 to 5V, 0 to 10V or user defined range between 0 and 10V. Each channel independently configurable by jumpers.
Offset error	Trimmable to 0 by potentiometer
Gain error	Trimmable to 0 by potentiometer
Differential nonlinearity	±1 LSB max
Integral nonlinearity	±1 LSB max
Monotonicity	Guaranteed monotonic
D/A pacing	Software paced
Data transfer	Double buffered software transfer, update on write to MSB register.
Throughput	System dependent, software paced.
Slew Rate	0.3V/µs
Current Drive (OP07)	±5 mA min
Output short-circuit duration	Indefinite
Output coupling	DC
Output impedance	0.1 Ohms max
Miscellaneous	Double-buffered output latches

Digital Input / Output

Digital Type (Digital I/O connector)	82C55 (not applicable on -P5 versions)
Configuration	2 banks of 8, 2 banks of 4, programmable by bank as input or output
Number of channels	24 I/O
Output High	3.0 volts min @ −2.5 mA
Output Low	0.4 volts max @ 2.5 mA
Input High	2.0 volts min, 5.5 volts absolute max
Input Low	0.8 volts max, −0.5 volts absolute min
Digital Type (Main analog connector)	
Output	74LS197
Input	74LS244
Configuration	4 fixed input, 4 fixed output
Number of channels	8
Output High	2.7 volts min @ −0.4 mA
Output Low	0.5 volts max @ 8 mA
Input High	2.0 volts min, 7 volts absolute max
Input Low	0.8 volts max, −0.5 volts absolute min

Counter section

Counter type	82C54
Configuration	3 down-counters, 16 bits each

Counter 0 - Independent, user configurable
- Source: Programmable - Internal 100 kHz or external (CTR0 Clock In)
- Gate: External (DIn2)
- Output: Available at user connector (CTR0 Out)

Counter 1 - ADC Pacer Lower Divider
- Source: 1 or 10 MHz oscillator (jumper selectable)
- Gate: Tied to Counter 2 gate, programmable source.
- Output: Chained to Counter 2 Clock.

Counter 2 - ADC Pacer Upper Divider
- Source: Counter 1 Output.
- Gate: Tied to Counter 1 gate, programmable source.
- Output: ADC Pacer clock

Clock input frequency	10 MHz max
High pulse width (clock input)	30 ns min
Low pulse width (clock input)	50 ns min
Gate width high	50 ns min
Gate width low	50 ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min

Environmental

Operating temperature range	0 to 50°C
Storage temperature range	–20 to 70°C
Humidity	0 to 90% non-condensing
Weight	11.2 oz. (320g)

9.2 CIO-DAS1602/16

Power consumption

+5	1.4 A typical, 2.1 A max

Analog input section

A/D converter type	ADS7805 successive approximation
Resolution	16 bits
Programmable ranges	±10V, ±5V, ±2.5V, ±1.25V, 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V
A/D pacing	Programmable: external source (Din0, positive edge) or internal counter (positive or negative edge, jumper-select able) or software-polled
Burstmode	13.3 µs
Data transfer	From 512-sample FIFO via interrupt, DMA, DT-Connect to external memory board or software polled
Polarity	Unipolar/Bipolar, switch selectable

Number of channels	8 differential or 16 single-ended, switch-selectable
Interrupts	2 to 7
Interrupt enable	Programmable
Interrupt sources	End-of-conversion, terminal count (DMA)
DMA	Channel 1 or 3
Trigger sources	External hardware/software (DIn0)
A/D conversion time	10 µs
Throughput	100 kHz
Differential Linearity error (Bipolar)	±1 LSB
Integral Linearity error (Bipolar)	±1.5 LSB
No missing codes guaranteed	16 bits
Gain drift	±7 ppm/°C
Zero drift	±2 ppm/°C
Input leakage current (@25 Deg C)	200 nA
Input impedance	10 MegOhms min
Absolute maximum input voltage	±35V

Analog Output:

Resolution	12 bits
Number of channels	2
D/A type	MX7548
Voltage Ranges	±10V, ±5V, 0 to 5V, 0 to 10V or user-defined range between 0 and 10V. Each channel independently configurable by jumpers.
Offset error	Trimmable to 0 by potentiometer
Gain error	Trimmable to 0 by potentiometer
Differential nonlinearity	±1LSB max
Integral nonlinearity	±1LSB max
Monotonicity	Guaranteed monotonic
D/A pacing	Software paced
Data transfer	Double-buffered software transfer, update on write to MSB register.
Throughput	System-dependent, software-paced.
Slew Rate	0.3V/µs
Current Drive (OP07)	±5 mA min
Output short-circuit duration	Indefinite
Output coupling	DC
Output impedance	0.1 ohms max
Miscellaneous	Double-buffered output latches

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- Source: Counter 1 Output.
- Gate: Tied to Counter 1 gate, programmable source.
- Output: ADC Pacer clock

Clock input frequency	10 MHz max
High pulse width (clock input)	30 ns min
Low pulse width (clock input)	50 ns min
Gate width high	50 ns min
Gate width low	50 ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min

Environmental

Operating temperature range	0 to 50°C
Storage temperature range	-20 to 70°C
Humidity	0 to 90% non-condensing

EC Declaration of Conformity

We, Measurement Computing Corp., declare under sole responsibility that the product:

Part Number	Description
CIO-DAS1600	ISA Bus, analog and digital I/O board

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

Carl Haapaoja, Director of Quality Assurance

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